5-2013

Automated testsystem of COGNISION headset for cognitive diagnosis.

Joshua I. White
University of Louisville

Automated Testsystem of COGNISION™ Headset for Cognitive Diagnosis

By

Joshua I. White
B.S., University of Louisville, 2010

A Thesis
Submitted to the Faculty of the
Speed School of Engineering of the University of Louisville
As Partial Fulfillment of the Requirements
For the Professional Degree of

MASTER OF ENGINEERING

Department of Bioengineering

May 2013

COGNISION™ Headset Automated Testsystem

Submitted by:_____

Joshua I. White

A Thesis Approved on

_____
(DATE)

by the Following Reading and Examination Committee

_____
Steven C. Koenig, PhD, Thesis Director

_____
Robert S. Keynton, PhD – Thesis Committee

_____
William D. Ehringer, PhD – Thesis Committee

ACKNOWLEDGEMENTS

Special thanks to these people for helping make sure this project could happen. K.C. Fadem, Ben Schnitz, Jorge Campos, Tommy Roussell, Dr. Ehringer, Dr. El-Baz, Dr. Keynton, Dr. Koenig and Troy Thielen, Jessica Freeman. These individuals gave me the opportunities for which I am grateful, and those experiences which have shaped my education that will lead to bigger and better things.

K.C. Fadem whose skills at organization and leadership have become my template to use for the rest of my life. Tommy Roussell, who was the first person to show me LabVIEW and has led to the past 4 year endeavor as I have acquired more and more competency with the programming platform. Dr. El-Baz for his infinite patience and guidance, and Jorge Campos and Ben Schnitz who have been my most important resources for learning about principles in electrical engineering.

Dr. Keynton, my undergraduate advisor, who helped guide me to my master's degree.

Dr. Koenig, my mentor for this thesis, for being there to guide me through any necessary hurdles these past 2 years.

Lastly Jessica L. Freeman, who has always been there for me, who helped me develop the discipline necessary to complete school.

ABSTRACT

There are more than 15 million Americans suffering from a chronic cognitive disability in the Unites States. Researchers have been exploring many different quantitative measures, such as event related potentials (ERP), electro-encephalogram (EEG), Magnetic Encephalogram (MEG) and Brain volumetry to accurately and repeatedly diagnose patients suffering from debilitating cognitive disorders. More than a million cases have been diagnosed every year, with many of those patients being misdiagnosed as a result of inadequate diagnostic and quality control tools. As a result, the medical device industry has been actively developing alternative diagnostic techniques, which implement one or more quantitative measures to improve diagnosis. For example, Neuronetrix (Louisville, KY) developed COGNISION™ that utilizes both ERP and EEG data to diagnose the cognitive ability of patients. The system has shown to be a powerful tool; however, its commercial success would be limited without lack of a fast and effective method of testing and validating the product. Thus, the goal of this study is to develop, test and validate a new "Testset" system for accurately and repeatedly validating the COGNISION™ Headset.

A Testset was constructed that is comprised of a software control component designed using the Labview G programming language, which runs on a computer terminal, a Data Acquisition (DAQ) card and switching board. The Testset is connected to a series of testing fixtures for interfacing with the various components of the Headset. The Testset evaluates the Headset at multiple stages of the manufacturing process as a

whole system or by its individual components. At the first stage of production the Electrode Strings, amplifier board (Uberyoke), and Headset Control Unit (HCU) are tested and operated as individual printed circuit boards (PCBs). These components are again tested as mid-level assemblies and/or at the finished product stage as a complete autonomous system with the Testset monitoring the process. All tests are automated, requiring only a few parameters to be defined before a test is initiated by a single button press, and then selected test sequences are begun for that particular component or system and are completed in a few minutes.

A total of 2 Testsets were constructed and used to validate 10 Headsets. An automated software system was designed to control the Testset. The Testset demonstrated the ability to validate and test 100% of the individual components and completed assembled Headsets. The Testsets were found to be within 5% of the manufacturing specifications. Subsequently, the Automated Testset developed in this study enabled the manufacturer to provide a comprehensive report on the calibration parameters of the Headset, which is retained on file for each unit sold. The automated test system's statistical analysis shows that the two Testsets yielded reliable and consistent results with each other.

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I. INTRODUCTION

A. Background

There are more than 15 million Americans suffering from a chronic cognitive disability in the Unites States; more than a million diagnosed every year with many of those patients being misdiagnosed as a result of inadequate diagnostics. (1-6) A majority of the misdiagnoses are due, in part, to the "soft science" or qualitative tools currently used for diagnosis, combined with a weak understanding by the medical community and device industry of the specific pathophysiologies that cause the disorders. Specifically, until recently, the available methods of diagnosis have included: imaging, psychometric testing, and electrophysiology techniques, which have been ineffective and possess low efficacy rates for diagnosing common cognitive disorders, especially Alzheimer's (Luck, 2005).

In cognitive disorders, imaging data is still considered to be qualitative since very few of the biomarkers available are analyzed computationally. Rather, images are viewed and analyzed by technicians and radiologists that look for specific changes known to be associated with a particular disease. Brain volumetry is a widely used quantitative method that calculates changes in volume of different brain structures (Fox, Freeborough, & Rossor, 1996).

Psychometric tests such as the Mini-mental State Exam (MMSE) measure memory and cognitive status in patients (Heinik, Solomesh, & Berkman, 2004). However, results from these tests can be difficult to discern since a number of these

patients also have additional difficulties in communication or movement, such as debilitations caused by stroke or other co-morbid conditions. In addition, conditions such as the testing environment where the assessment tool is administered or the number of times it has been administered can influence and bias the results as well.

In the area of cognitive electrophysiology tools, a few medical device companies have recently focused their attention on utilizing quantitative measures to improve the accuracy, reliability and repeatability of their cognitive diagnostic tools. For example, Neuronetrix (Louisville, KY) has developed a new system, the COGNISION™ Headset, which uses the electrophysiological-based parameters of electroencephalograms (EEG) and Event Related Potentials (ERP) to diagnose cognitive disorders. The Neuronetrix system has produced promising results in early clinical trials (Fadem, 2008). However, it has many functions and features that must be evaluated prior to consumer use. With the lack of availability of an automated platform for validation and verification of this cognitive diagnostic tool, quality control and performance evaluation of each Headset has been cumbersome and time consuming, which has limited the commercialization of the Headset.

B. Purpose of Study

The purpose of this project was to develop an automated software platform (utilizing the LabVIEW™ graphical programming language) that requires minimal user interaction from start-to-finish of the test, but with the capability to accurately, reliably and repeatedly validate the performance of each Headset in compliance with FDA regulations.

C. Hypotheses

Repeated testing of an individual unit will yield results whose difference between trials are not statistically significant.

Testing an individual Headset unit on two independent Testsets will not yield results whose difference is statistically significant.

D. Significance of Study

The ability to validate and test medical equipment to ensure valid results is a high priority to minimize inaccurate diagnoses and to aid in the quality of care of patients suffering from cognitive disorders. The Testsets produced in this project and the automated software that drives them will be used to test a new, promising clinical diagnostic tool in a cost effective and time efficient manner. As a result, the performance accuracy and reliability of the Headset will improve the quality control of the system and contribute towards improving the accurate diagnosis of cognitive disorders.

II. LITURATURE REVIEW

Patients suffering from cognitive decline can become frustrated in not knowing the cause, whether it happens slowly as part of the natural aging process or as a rapidly accelerated process caused by disease. Similarly, those born with cognitive disorders, typically have the ability to conceive of a normal life and suffer the additional hardship of perceiving what the "norm" is for the rest of the population. To ease the psychological pain experienced by these patients, better diagnostic and therapeutic methodologies must be developed. The focus of this chapter will be on identifying the: 1) different types of cognitive disorders; 2) current technologies commercially available for diagnosing these disorders; and, 3) different techniques implemented for validating and verifying performance of the cognitive diagnostic tools.

A. Cognitive Disorders

More than 15 million Americans are suffering from a chronic cognitive disability in the United States (1-6) and represent a huge cost both in terms of individual happiness/comfort and monetary loss to the individual and society as a whole. These conditions range from a life long struggle starting in childhood to debilitating and progressive diseases with cognitive decline until death. Some common forms of cognitive diseases can be seen in

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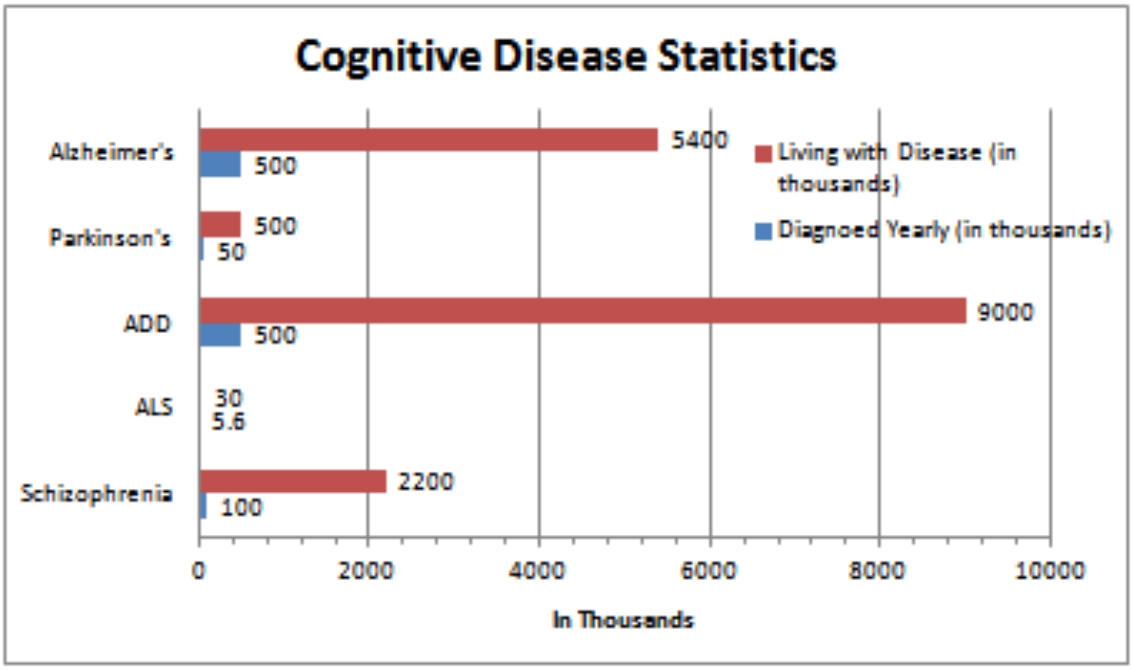


FIGURE 1 : USA Yearly Population Statistics For Common Cognitive Diseases (In Thousands) Showing The Prevalence Of The Diseases In The Current Population And The Number Diagnosed Each Year.

The common forms of cognitive disorders in children include attention deficit disorder (ADD) or attention deficit hyperactivity disorder (ADHD), Autism, and Down syndrome. ADD/ADHD is a disorder characterized by the patient's inability to control their attention on a subject matter, commonly in conjunction with poor impulse control, and seemingly a lack of attention to detail. Pathology stems from anomalies in dopamine pathways related to the "reward center of the brain." According to epidemiological data, approximately 4% to 6% of the U.S. population has ADHD (Jaska, 1998).

Down syndrome is caused by a genetic defect and the syndrome is generally apparent from birth. It has an easily distinguished phenotype and can cause significant mental retardation. Unlike many of the other diseases, methods of diagnosis are not the primary concern for Down syndrome; current research is pursuant of quantitative cognitive measurements to improve the understanding of drug efficacy. (Cano et al.,

2010) Measurements related to cognitive performance are taken before and after administration of drugs that hold promise for improvement of the deficits associated with Down syndrome.

Autism is a developmental disorder that appears in the first 3 years of life, and affects the brain's normal development of social and communication skills. The severity of the disorder can impede the ability for education and cognitive assessment. Like Down syndrome, there is a great need for the ability to quantify the cognitive function of the affected patients ("Alzheimer's Disease Facts and Figures," 2010).

Chronic cognitive disabilities have been occurring in adult patients at an expanding rate from factors such as the increase in life expectancy and improved health care from the mid 70's to present, which has lead to an exponential increase in cognitively impaired adults. The number of age-related cognitive deficient adults will probably continue to increase until 2050 as a result of the aging baby boomers population and increasing life expectancies; at that time, more than 1 out of 5 people will be over the age of 65 (Obeso et al., 2008). In the aged population, cognitive disabilities are caused by the onset of cognitive diseases, such as Alzheimer's, Parkinson's or part of the natural aging process.

Alzheimer's disease is characterized by slow brain cell death from beta amyloid plaque burden and tau. The first outward signs of the disease are forgetfulness which makes memory and cognitive function the current target for early detection (Obeso et al., 2008). Parkinson's disease consists of the death of mid-brain dopanergic secreting neurons, resulting in lower amounts of dopamine reaching their target receptors; thereby, causing a decline in the individual's ability to control voluntary muscles (Michael J. Fox

Foundation, 2012). Research is ongoing in determining why the later stages of the disease exhibits cognitive decline (National Institute of Neurological Disorders and & Stroke, 2004)(Schizophrenia.com, 2010).

Schizophrenia – disease characterized by paranoia, delusions, hallucinations and a detachment from reality (Robi Polikar et al., 2008). A lifelong disease usually starting between the ages 18 and 30, it manifests from mild to acute, and can distort memory and normal cognitive behavior. This disease's prevalence is roughly 1 in 100 adults. (Robi Polikar et al., 2008) Cognitive Diagnostic Modalities

With the increasing number of people being affected by these diseases, it is becoming of critical importance that accurate diagnostic techniques be implemented. However, the majority of diagnostic methods currently used are based on "soft science" or more qualitative approaches. As a result, in the case of Alzheimer's for example, there is a low efficacy percentage of diagnosis, about 75 % (R. Polikar, Greer, Udpa, & Keinert, 1997). Thus, many patients are diagnosed as either false positive or false negative with the disease. Subsequently, many patients receive, or do not receive, the appropriate treatment for their disease case. Lack of early detection or proper diagnosis often times results in an unnecessary cognitive decline in the patient before effective treatment can be applied.

Currently, there are a variety of modalities that have been used for diagnosing and assessing the cognitive and physiological state of the brain. The primary diagnostic modalities include: 1) imaging methods, which give an excellent spatial understanding of disease pathology and clearly show morphological changes; 2) cognitive assessment methods involve questionnaires and quizzes to stress the various cognitive functions and

elicit standard responses; and, 3) electrophysiological methods, which provides great temporal resolution, but poor spatial resolution. Great temporal resolution (Casey, 2011) s to changes that are observable on the order of milliseconds, where as poor spatial resolution (Millet, n.d.) s to difficulties in determining where exactly in the brain the signal originates. Research has been done for each type of modality (described below) along with the development of specific biomarkers that correlate with the disease(s) in question.

B. Imaging Methods

Imaging methods such as Computer Tomography (CT), Magnetic Resonance Imaging (MRI), and Positron Emission Tomography (PET) are able to show the physical changes that occur with disease. CT is used to generate anatomical images of the body. It does this by passing a body through a donut shaped machine, an x-ray emitter and collector then whirl around the inner circumference of the ring at high speed and collect information as the body is passed through the center. The computer reconstructs the image as coronal slices, which can then be rendered into three dimensional images of the body. Similarly, MRI also focuses on anatomical features; however, the mode of operation is different. MRI uses a power magnetic field and electromagnetic pulses at the resonance frequency for hydrogen nuclei. Once affected some of the nuclei will release their own photons at the varying densities depending on their concentration in the tissue, i.e. the water concentration of the tissue. The reconstruction is the same as for MRI images once the signal has been collected. Separately, the primary purpose of PET imaging is to determine the physiological functionality and activity of specific regions of the body under investigation. PET relies on radioisotopic decay of an injected or

ingested material. As the isotope decays it releases the radioactive particles and they are collected by a scintalator much the same as the MRI and CT collect their signals. Just like the MRI or the CT, the images are reconstructed from the signal.

Both MRI and CT can detect certain cognitive diseases via brain volumetry and they both have comparatively high spatial resolution as opposed to other imaging methods. In brain volumetry, the brain is imaged, a 3D model is constructed and voxels (3D equivalent of pixels) are used to gauge the volume of specific brain structures under investigation (Zakzanis, Graham, & Campbell, 2003). In Alzheimer's disease, for instance, there is a significant decrease in volume of all brain structures over time, particularly the hippocampus early on (Hostetler et al., 2011). However, while there is a positive correlation between brain volume and certain diseases, the likelihood of a false positive is significant since many perfectly normal, healthy geriatric patients also have brain shrinkage and do not exhibit cognitive decline (Fox et al., 1996).

Meanwhile, PET imaging has a fairly low spatial resolution in comparison to MRI and CT, but has made progress in positively identifying persons with a beta-amyloid plaque burden (Drzezga et al., 2008)(Wind et al., 1997). This method also has a tendency to yield false positives, since all persons with Alzheimer's have a substantially higher than average amount of beta-amyloid plaque accumulation. However, not all persons with beta-amyloid plaque accumulation have dementia. With all the types of imaging techniques implemented thus far, disease detection is limited in the pre-dementia and mild impairment phase, since insufficient damage has occurred to be identified in the images.

C. Psychometric Methods

The psychometric tests fare better than the imaging techniques listed above at assessing cognitive function, but have a number of drawbacks. There are many of these tests and some physicians use them as a routine diagnostics, however, each test targets and analyzes very specific pathways of the brain to ascertain if those sections of the brain are working correctly. There are hundreds of published psychometric tools, but for evaluating memory the MMSE has been adopted by many physicians as well as being incorporated into the Alzheimer's disease Neuro-imaging Initiative (ADNI) protocols for diagnosing Alzheimer's (Casey, 2011). Although these tests have been developed to do their best at eliminating exogenous variables; they are affected by the test giver's demeanor, patient alertness, patient disposition, and outside distractions. A test subject may have highly variable test scores from one week to the next, making disease correlation difficult from these various factors. Also, cognitive tests of this nature *cannot* be repeated frequently as the subject "learns" the test, so their performance will improve from practice or decrease from boredom as a function of frequency and total number of tests given, giving unpredictable results (Steinmetz, n.d.)

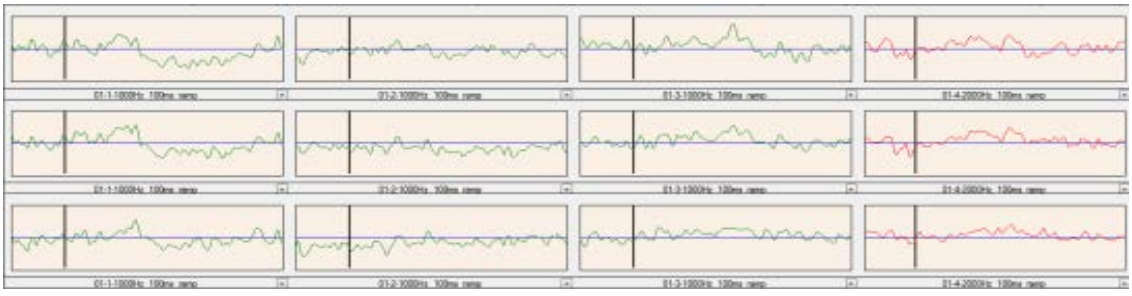


FIGURE 2 : View Of Four ERP Epochs From Three Channels. Each Epoch Is A Stimulus Response EEG About One Second Long. The Blackvertical Bar Represents When The Stimulus Occurred.

D. Electrophysiology Methods

Another method for evaluating cognitive ability is electrophysiological testing. There are several types of electrophysiological signals which have been used to date to evaluate cognitive ability including, magnetic encephalograms (MEG), electroencephalograms (EEG) and event related potentials (ERP). An EEG is performed by placing electrodes on the scalp and monitoring the brain waves produced by the test subject (FIGURE 2) The waves emanate from the changing of the average polarity of a region due to neuronal activity. With help from low impedance amplification, the microvoltages collected at the scalp can be amplified to voltages capable of being digitized and recorded by a computer. The MEG techniques can be utilized the same way as the EEG techniques, however the cost of building the collection arrays are magnitudes more expensive. MEG detectors are as large as MRI and CT scans, making them unportable. MEG works by picking up the magnetic field changes, these signals are attenuated a great deal more by distance than EEG, but are less distorted by the skull, and therefore provide better spatial resolution than that of EEG.

ERPs are created by repeatedly subjecting the test subject to a stimulus: light pulses, images, sounds, vibrations, etc., and then collecting the time locked brain waves that follow (either EEG or MEG). Time locked signals refer to the coordination of the signals in relationship to each other and the high precision system clock that keeps track of when the signal was produced. These time locked signals are then overlaid upon one another and averaged for each sample time starting with the time of the initial stimulus. Any brain waves not related to the event related stimulus will average to zero (FIGURE 3), leaving only the signals associated with the patient's response to the stimulus (Luck, 2005). These signals have unique characteristics depending on the stimulus paradigm

which can be analyzed to yield probabilities for different diseases using a trained classifier to examine wavelets, latency, amplitude, polarity and other features (R. Polikar et al., 1997).

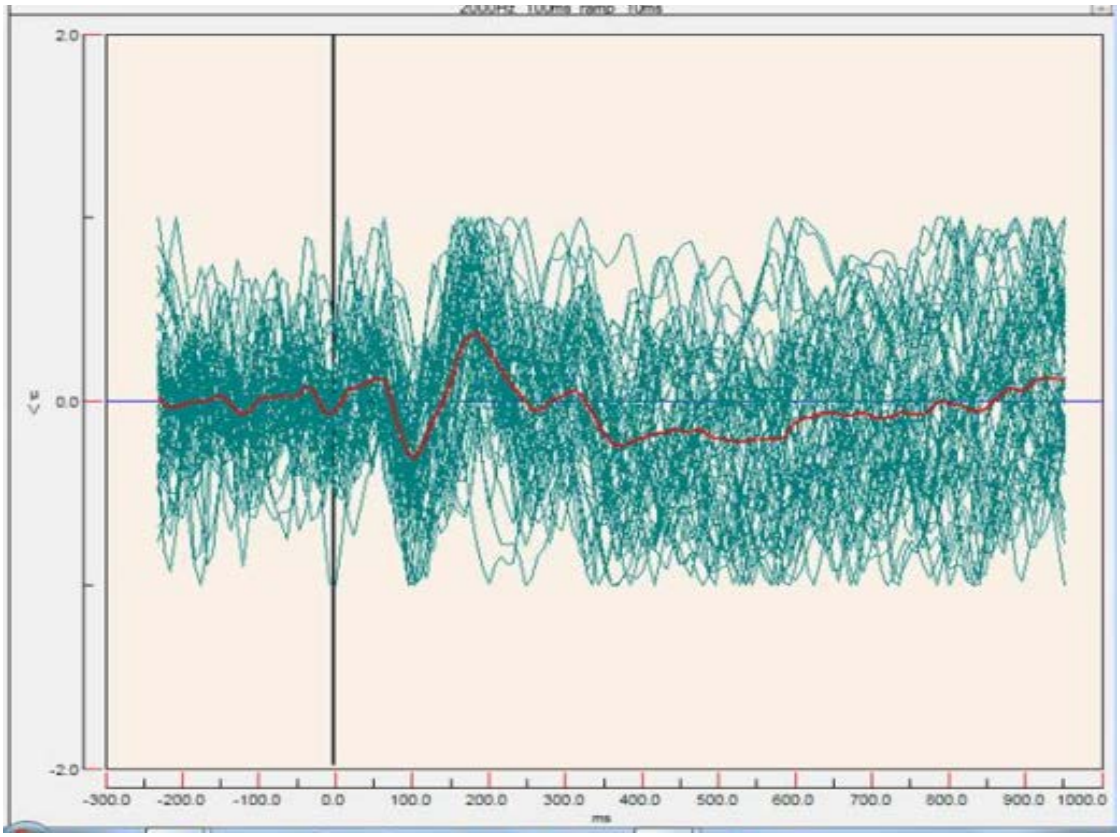


FIGURE 3 : Single Data Channel Showing 100 Overlaid ERP Epochs (Blue-Green) And The Average Of The Epochs (Red). The Peaks At 200 And 300 Ms Are Tell Tale Peaks Used In Alzheimer's Detection.

The benefit of using ERP over other forms of cognitive assessment is that it allows monitoring of the precognitive *and* cognitive responses to stimuli. When a stimulus is imposed, there are brain waves generated by other areas of the brain leading up to the moment when the cerebral cortex (the part of the brain responsible for cognitive comprehension) receives the information. The significance of precognitive activity is

that the patient cannot influence the results of the stimulus; making it an additional independent measure of brain activity unaffected by the subject's thought processes. The brain wave's features associated with these diseases are unique; thus, a powerful computer in conjunction with a trained classifier and quantitative analysis method can yield reliable pass/fail results when testing for a specific disease.

Unfortunately, unlike the panacea of cognitive assessments and brain imaging modalities, electrophysiology methods have not been as widely accepted as a tool for clinical diagnosis as other modalities other than for sleep and seizure studies. Their use in determining cognitive disorders is rare in a clinical environment due to the lack of dedicated ERP systems and problems, thus far, with comparable results from lab-to-lab and the need for specially shielded rooms. EEG setups have been traditionally customized by individual labs using software and custom stimuli to record the ERPs. As a consequence of this, it has been difficult to compare data from one lab to another as no two labs had the same equipment, or the same test paradigm. Unlike imaging modalities, which simply take a picture of an existing structure, ERPs actually evoke, via a specific stimulus, a distinctive response. Unless the stimulus is the same from one test to the next, and one lab to another, the response will not be comparable, so a common designated biomarker cannot be easily identified.

E. Neuronetrix COGNISION™ System

Recently, a dedicated ERP system has been developed, COGNISION™ (Neuronetrix, Louisville, KY), and is currently being evaluated in clinical trials. The COGNISION™ Headset (hereafter referred to as Headset) allows ERPs to be collected in clinical settings with a high level of accuracy and little variation from laboratory to

laboratory or between devices (Swaminathan, Mohan, & Arunachalam, n.d.). The Cognision Headset is a handheld, wireless, ambulatory, ERP device for the diagnostic of cognitive disorders. It is designed specifically to perform ERP tests and their ability to produce biomarkers associated with cognitive disorders.

F. Validation and Testing

As with any medical device, ensuring a device is robust, safe and effective is of paramount importance and is achieved through the implementation of proper validation and testing procedures. The consequences of releasing an un-validated device into the market can be dangerous, even fatal, in instances where electrical shock is possible, e.g. open brain or heart surgery, and subcutaneous catheterizations (Reid, 1978). The FDA requires that medical devices be tested and validated to ensure they are safe and effective to gain approval for clinical use and sale [CFR21 Part 11 and Part 820](22). The FDA does not provide a strict requirement about how the validation and verification processes are performed, so the scope of methods implemented by companies vary from the simple use of statistical methods, where only a small percentage of devices are tested, to the use of robust, fully-automated techniques developed by the respective, individual company.

Currently, laboratories evaluate EEG and ERP systems via a manual process using individual pieces of electronic testing equipment such as oscilloscopes, function generators, and custom built hardware. Measuring parameters as simple as frequency response or gain linearity can take an hour each. Some test systems exist, such as the FLUKE Medtester series, which is primarily a Biosignal generator used to test EKG devices; however, these testers are limited because they lack the ability to test equipment with complex functions and built in firmware, such as those found in ERP devices.

III. INSTRUMENTATION AND EQUIPMENT

A. Cognision 3000 Headset

The COGNISION™ System (CS) consists of a ten-electrode headset and control unit (Figure 4a) with signal conditioning (Figure 4b) to measure EEG and ERP for non-invasive, early-stage detection and diagnosis of clinically-significant neurological disorders. The CS concept leverages clinically-accepted diagnostic ERP technology to record the electrical activity of a patient's brain waves (typically 100 μV pk-pk) while the brain is stimulated to perform cognitive tasks that are specific to the cognitive disease being tested.

FIGURE 4 : The COGNISION™ 3000 Consists Of (A) Ten-Electrode Headset, (B) Control Unit, And (C) Data Acquisition. The Uberyoke (1. White Box) Contains Electronics For Signal Amplification, Analog-To-Digital (A/D) Conversion, And Control Logic (C).

Advanced signal processing techniques are applied to these data to elucidate the possible disease state(s). Pattern recognition software is used to identify disease specific biomarkers associated with specific regions of the brain that are linked to cognitive performance. The trained cognitive classifier assesses the probability of a disease by comparing morphological features of the patient's recorded brainwave activity during

cognitive testing to a database of brain waveforms with characteristic features associated with a variety of cognitive disorders.

The CS offers many technological advantages and clinical benefits compared to other commercially-available ERP devices. First, current ERP devices are large in size and weight requiring transport within the hospital environment on carts. In contrast, the CS is a portable, light-weight, handheld device. By leveraging electronic miniaturization and advances in cell phone technology, a personal computer (PC) and data acquisition system have been replaced by a unit that fits in the palm of the hand.

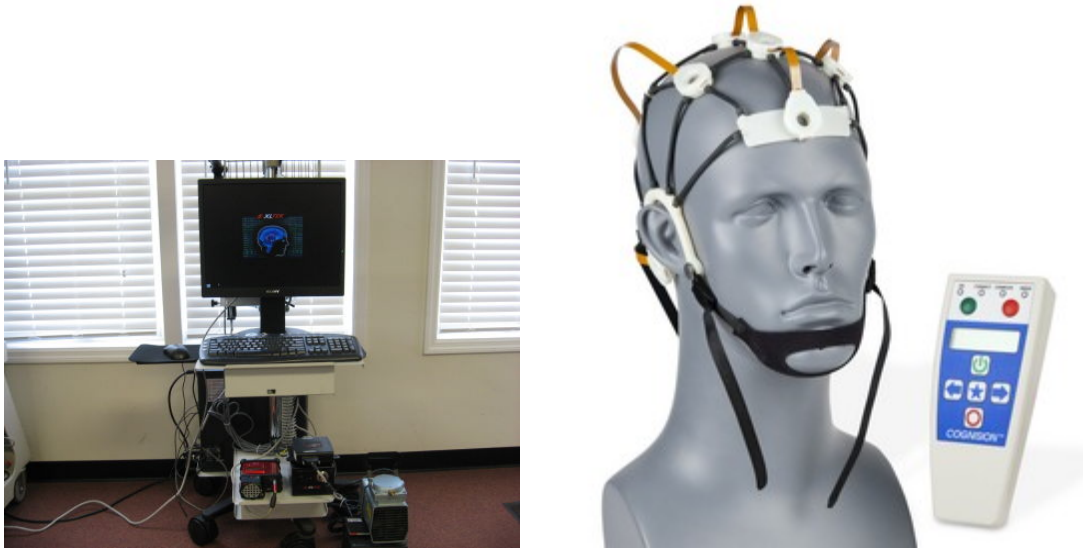


FIGURE 5 : XLTEK Design, Notice The That It Requires A Cart To Mobilize The Equipment (Left). COGNISION™ The Small Size Makes It Far More Portable (Right).

These improvements enable clinicians to use the CS in remote setting(s), which were previously inaccessible (i.e. sports arenas, battle fields, and EMS ambulatory units). Second, the CS is wireless allowing for untethered communication, and data transfer, allowing physicians and support staff to monitor test subjects from a separate room without disturbing them. The CS uses active electrodes for EEG measurements, which

can be used in conjunction with integrated circuits (IC) to perform specialized tasks. For example, real-time impedance verification is used to continuously monitor and validate that the active electrode maintains a low impedance electrical contact with the patient. Current ERP devices employ 'passive electrodes', electrodes that do not contain any electronics, the electrodes can often become disconnected during cognitive testing without any indication and that can result in aberrant or corrupt data. Additionally, the CS signal conditioner is designed with unity gain (signal buffering) to minimize signal degradation between the electrode and the amplifier for better signal-to-noise ratio (SNR). The CS Headset continually samples electrode impedance, monitors for artifacts, and ensures all cognitive test sequences are completed and sample data recorded.

FIGURE 6: Hydrodots Seen From Various Angles. The AG/AGCL Tabs Of Each Hydrodot Articulate With A Metal Contact Ring In Each Electrode Pod. The Gel End Of The Dot Articulates With The Patient Scalp.

Hydrodot™ electrode contacts are used for maintaining electrical continuity between the sensing electrode and patient. The current clinical practice involves the use of a blunted needle to abrade the patient's scalp (preparation) and apply saline or electrolytic gel (coupling) to acquire the voltage potential at the electrode placement site. This procedure can be uncomfortable, sometimes painful, and messy. In contrast, Hydrodots™ (Figure 6) are a gelatin electrolytic pod that maintains its shape, and

provides superior physical contact and silver/silver chloride contact electrical coupling to acquire higher-fidelity EEG waveforms. These special features and unique electrodes make the system more complex for testing than other EEG/ERP test systems, and require a sophisticated tester to ensure the highest quality products.

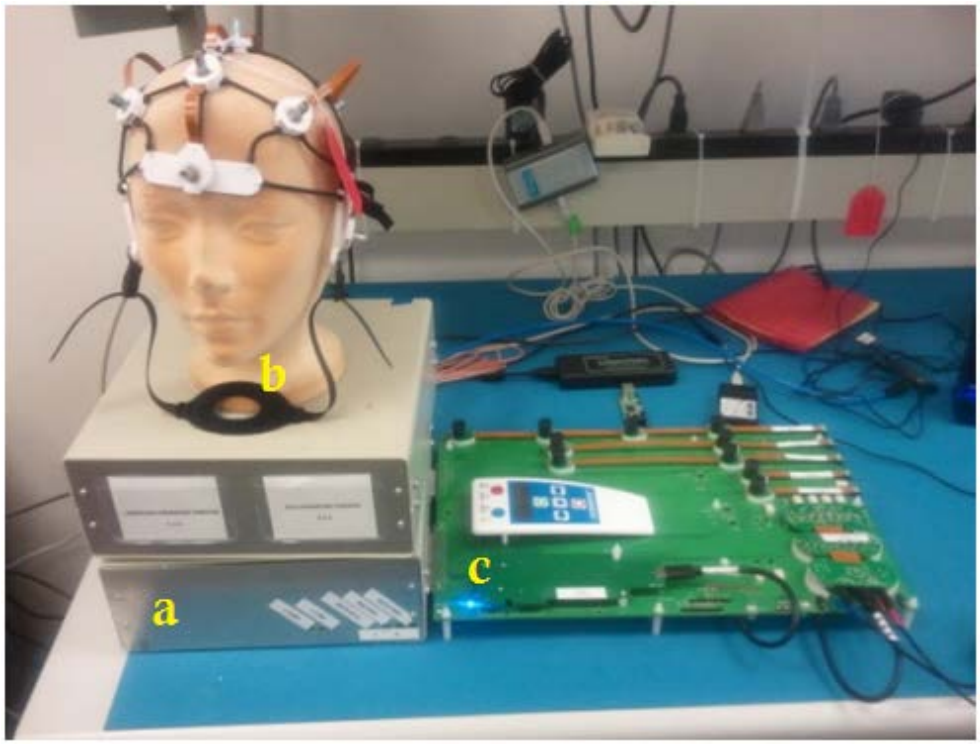


FIGURE 7 : CS Testset, On The Left The (A.) MSBB And (B.) Testhead, The Right Side Of The Image The (C.) Testboard Which Is Currently Populated With A CS 3000 System Ready For Testing.

B. COGNISION™ Testsest

The physical Testset is a proprietary hardware device for testing the Headset. The complete Testset (hardware and software) is an automated test fixture with the ability to test the Headset at each stage of Validation and Verification testing during the manufacturing process. The Testset includes a software control component designed on

the National Instruments LabVIEW platform using the LabVIEW G programming language, which runs on a computer terminal and a Data Acquisition (DAQ) card + switching board. The "Magical Switching Bio-signal Board" or MSBB (as termed by Neuronetrix) connects to a series of test fixtures for interfacing with the various components of the Headset.

The Testset can simulate the Headset HCU to test entire system(s) or individual component(s). There are 14 separate configurations (see appendix c, section 7) that allow trained technicians to test each component against a known test standard, or use the component independently with the Testset to simulate the entire CS 3000 system. For example, an Uberyoke can be placed on the Testboard with a set of "golden" strings (term indicating calibrated and validated electrode strings used as standard) and the Uberyoke's circuitry tested by subjecting it to analog tests and executing its firmware commands to control its digital switches. Analog tests such as: power consumption, baseline noise, Cal tones test (calibration tones used for measuring impedance while an ERP test is in progress), frequency response, gain linearity, and cross talk can be performed via the custom software interface.

The Testset allows a variety of test to be performed in an automated fashion. There are noise level tests, noise sources from both internal components of the Headset and from electrical magnetic interference (EMI), and baseline noise values external to electrodes. The frequency response, common mode rejection ratio (CMRR), cross-talk, and gain linearity are all tests that are incorporated into the single automated test suite; allowing the press of a single button to pass or fail individual pieces of equipment or entire Headsets.

1. DAQ Card Control

The (Data Acquisition) DAQ card (Ue9 Labjack, Denver, Colorado) (FIGURE 8) has many features and functions for collecting and generating signals. Universal asynchronous receive/transmitter (UART), serial port interface (SPI), Streaming DAC out, streaming analog signals in from the Kelvin circuits (current monitoring), and Digital Input/output for switches that are distributed throughout the MSBB (magical switching Biosignal board. The DAQ card is the single most important piece of hardware as it serves as the interface between all the various switches and parts in the Testset, and the computer. This data card needed to have communication channels for SPI and UART, (industry standardized communication protocols that exist in the Uberyoke and HCU). It also required analog inputs and outputs, for simulating waveforms and monitoring the voltage output of the current monitors. The digital I/O (DIO), although not enough to drive all the switches on the board, was required to drive the port expanders.

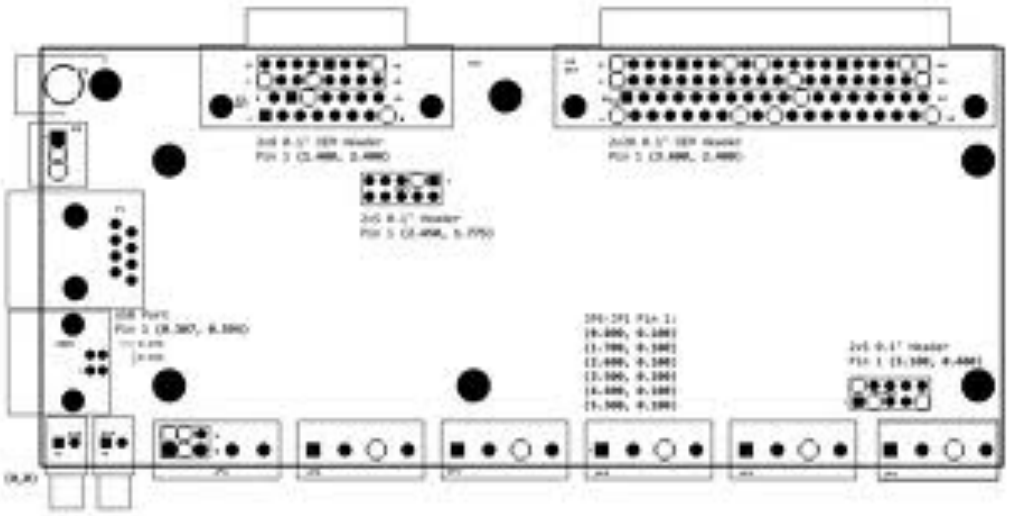


FIGURE 8 : Labjack Ue9, the DAQ card and "brains" of the testset. It functions as the interface and programmable circuitry that drives all the switches in the Testset.

The Labjack is the brains of the Testset; it is the controller for all of the switches in the MSBB. The DAQ card serves as the interface between the computer and the rest

of the hardware. It generates the Biosignal, has the firmware necessary for interpreting the information sent from the computer to control switches, and communicate with the various chips and peripherals.

2. Port Expanders

(MCP23S08, Microchip Technology INC., Chandler, Arizona) The DAQ (Data Acquisition) card did not possess enough Digital I/O ports (DIO), requiring a port expander chip to be used. These port expanders give a system an expanded ability to control a greater number of digital switches. This is necessary because there are not enough ports on the DAQ card to control the MSBB. (For a comprehensive list of switching needs, see PS-1487, section 7.4). Several of these chips were used to provide the necessary switching capacity in the MSBB. There were a total of 12 additional DIO added with the use of the port expanders.

The chip uses a 4 wire communication protocol called SPI (Serial Peripheral Interface). The DAQ card had driver level function calls for operating 4 of the digital channels (DIO0 - DIO3) as SPI lines. The port expander was prototyped on bread boards and controlled with the DAQ card. In using the chips the first step after wiring them correctly is to initialize the registers. The initialization procedure defined by the manufacturer in the chip specification did not work according to specification. The specification for the communication protocol for the SPI did not mention how to properly initialize the chip, the first register had to be written twice, to be responsive. Several additional registers were required to be set for the chip to perform for this application. The registers are responsible for port direction (R/W), Port polarity (inverted/normal), port state (high/low) and whether the chips responded to all commands or only

commands that are specifically addressed to them with a two bit code. The addressing register was set last, since it resulted in the initialization needing only to be sent globally instead of addressing each chip individually; resulting in a 75% reduction in the amount of time necessary to initialize them. The DAQ card's SPI channels only output 3.3 volts, but the operating voltage for the port expander is 5V. As a result, a level shifter (Schmitt trigger) was required to shift from 3.3 to 4.5 volts.

3. Kelvin Circuits

Kelvin circuits infer the current draw of a particular component by comparing the voltage at two different points along the VS for a particular component. They make it possible to determine if a short or an open is occurring when a component is placed on the Testboard. Uberyokes, HCUs, and electrode strings all have a known nominal current draw and deviations from these numbers are flagged for investigation. These are sampled with the Testset's analog inputs and a switch in the Labview application was designed to enable sampling of those ports and report them in a graph.

C. Testhead

The test head is a fixture for testing the device as a finished assembly. The Headset is mounted on the Test Head with an emitter post for each electrode and signals are then fed to the electrode posts. The Test Head is a modified Styrofoam display head for selling wigs and hats. It has ten electrode post made from sections of brass pipe, each pipe has a flexible rubber column with a screw inserted through it and a copper braid attached. The copper braid serves as a flexible conductor for making contact with the Monel ring of the electrodes. Once the Headset is in place, the screw is tightened and the rubber tube, bulges out, causing the copper braid to articulate with the Monel ring of the electrode.

FIGURE 9 : Testhead, A Fixture Of The Testset Wearing The COGNISION Headset. This Fixture Is Used To Test The Headset Once It Is Assembled And Completed Systems. It Allows The Simulated Biosignal To Be Injected Into The Electrodes With Conductive Post That Articulate With The Electrode Pod's Monel Ring.

D. Testboard

A test fixture, this is the actual interface between the hardware to be tested and the hardware of the Testset. The Testboard functions as the distribution highway for all the signals of the MSBB and Headset. It has only a minimal amount of active circuitry on it, with the idea that any changes to the Headset or degradation of the Testset will occur with the Testboard; it can be easily redesigned, and repaired. When designing the Testboard the major consideration was EMI. The signals output to the Headset are in microvolts and these signals have to be shielded with ground planes and spatially isolated to prevent noise from entering the conductors.

FIGUER 10 : Test Board With 1.HCU TOP, 2.HCU BOTTOM, 3.Uberyoke, And 4.Electrode Strings In Position. This Is A PCA Test Fixture That Allows The Unassembled Components Of The CS System To Be Mounted And Tested.

The baseline noise of this system is as low as 500 nano-volts. The Bluetooth emitter on the HCU had to be placed as far from non-digital signals as possible to prevent

interference. The only circuits that are located on the Testboard are solid state switches, and the Kelvin circuits.

E. Oscilloscope

A Tektronix oscilloscope with 100 MHZ bandwidth and 1 GS/s sample rate, it has standard features, 12 automated measurements, and context-sensitive help (Figure 11). The various features allow signals to be monitored as it progresses through the Testset, and to determine the appropriate voltages of the inputs and outputs. The o-scope was used during prototyping and to validate the test set. See Appendix B PS-1487 section 7 on validation for more information.

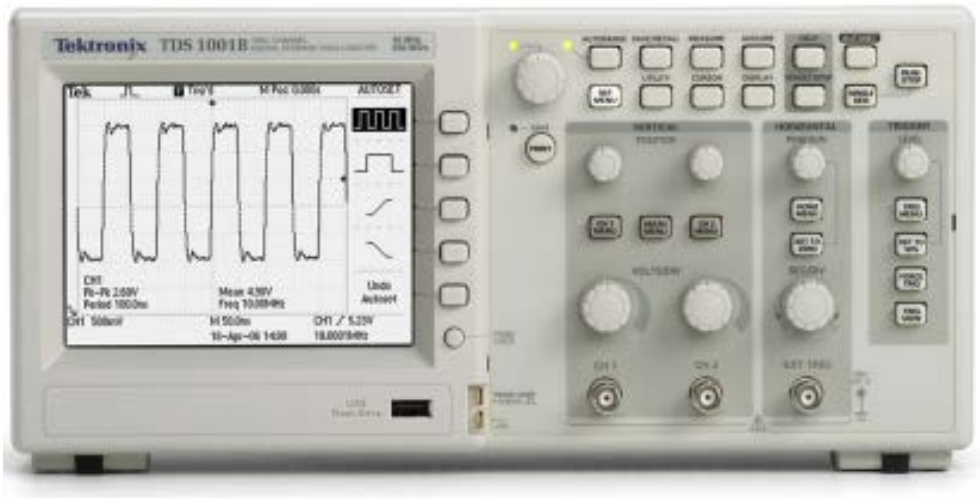


FIGURE 11 : Tektronix Multifunction Oscilloscope. This Was The Principle Tool For Validating The Testset As Well As Testing Its Circuits During Research And Development.

F. Function Generator

A Function generator (BK Precision) with variable DC offset, 4 digit LED display, course and fine tuning; it can produce sine, square, triangle, pulse, and ramp outputs (FIGURE 12). It's range is 0.2 Hz to 5 MHz in 7 ranges. This piece of equipment was primarily used to validate the Testset's signal input and output. See Appendix B PS-1487 section 7 on validation for more information.

FIGURE 12 : BK Precision Function Generator, Used To Produce A High Fidelity Signal And Validate The Signal Generator In The Testset

IV. PROCEDURES

A. Device Design

User Needs – A list of test were generated by itemizing the subsystems. A test was created for each subsystem. A basic consideration that helped to generate the specification was how to accomplish the tests that needed to be performed. (For a complete detailed list of design specifications see Appendix B section 7 PN-1487 section 7 SPECIFICATIONS) Prototyping (see PS-1487 Section 5 Block Diagram for hardware flowchart)

B. LabVIEW Application

(LABVIEW 11.0, National Instruments, Austin, Texas) Developing a (LabVIEW Virtual Instrument) VI for access to the virtual serial port with the Bluetooth Technology was necessary to test communication with the HCU. A Bluetooth Development Board (BDB) by Ezurio (Model number omitted) was utilized as a learning tool for communicating and interacting with the Bluetooth interface. LabVIEW currently does not have a function or module for pairing with Bluetooth devices. Instead, a third party library, 32feet-in-the-hand, which is an open source technology that allows pairing with a Bluetooth device. After pairing with the device a virtual com port was allocated to enable serial communication with the device. Once the Bluetooth device was paired and

a port set up, a standard serial communication protocol was all that was required for communication with the device via ASCII or hex commands.

C. Labjack UE9 DAQ Card

The first step to controlling the Testset was to learn how to communicate with the UE9; it has an USB connector and an Ethernet connector. It was established that the Ethernet communication would allow for more flexibility in control, as the Testset could then be controlled from anywhere and to anywhere provided there was network access. Low level VI functions were designed to access each port both digital and analog, and communication protocols such as SPI and UART.

D. MSBB (Magical Switching Biosignal Board)

This board interfaces between the Labjack and the Testboard. It contains all the switches, and signal conditioning elements necessary for testing the board with the exception of the components that have restrictions on the length of their conductors, i.e. CCS –ICDU64 programmer and the Kelvin circuits. The ports on the Labjack and interfaces can be used to turn the switches on and off to redirect signals and talk to the chips. After the basic input output functions were finished, sub routines were made to control the switches, such as initialization, and state machines.

E. Test Design

(See section 9 of PS-1487 of Appendix B)

The tests were designed with a common template in mind: Initialize Testset -> Get User input-> Perform Test -> Test data for Pass/Fail -> Generate report. The

Graphical User Interface (GUI) also had a template design, with the user controls on the left and the indicators on the right; with common controls and indicators between tests. A common theme for button colors, shapes and sizes were also used (Example screenshots of the GUIs can be seen in PS-1487, section 9). Error monitoring and stop buttons were incorporated into each tests, the testset hardware was designed to prevent any states from causing damage, but having a stop button to terminate the execution of a test saves time in the instance that a test needs to be reset.

Each test had a unique task to accomplish, using a common test pattern. Each test required data collection for some number of samples, and with some parameters. Either a single one shot data collection (single sample set) or a loop that varied a parameter such as frequency or gain. The Frequency Response Test and Common Mode Rejection Ratio (CMRR) test both required a loop to run that varied the frequency and kept the amplitude constant, because of this both test were incorporated into the same panel, a single switch in the MSBB would short all the inputs to each other for the common mode. The Gain Linearity Test required constant frequency with varied amplitude. The same loop structure could be used for all three tests with a different formula for each loop structure that regulated frequency, amplitude, and number of samples. The crosstalk-noise test only differed in that in the crosstalk test there was a signal being injected to one electrode at a time. For this test, the loop process is nested inside a of a larger loop that controls the channel that is open. For a full description of each test see Paragraph (0 of section 0IV Procedures.

Tests required pass fail parameters to determine the pass/fail criteria for the received signal amplitudes and frequencies. The method used to measure was identified

and implemented. Tests required built in LabVIEW tools for detecting frequency, amplitude, peaks, and rms. The criteria can be seen in the example test system report of Appendix-B.

F. Validation of the system

1. Data Validation

The Testset and tests were validated systematically and incrementally. The first steps were to validate the Testset to make sure all the individual components were performing as expected. As an example, when a signal was set in the application to 400 μV, a voltage of 2.5V is expected to be at input of the voltage dividers (See PS-1487 section 7, Appendix B for example values). Several test points were added during the design phase, all with expected values to help validate the system. Voltages and frequencies at each test point were tested, to ensure that the values match expectation. As an example: The output of the DAQ card was 0 to 5V which was ultimately divided to a dynamic range of -400 to 400 mV, with a resolution of 12 bits, a sensitivity of 97 nV. Then when the tests were performed, the same procedure was repeated, this time probing the test points monitoring the changes in the values as the test progressed. Other test points allowed the observation of digital signals. Visual inspection of the signals were used to make sure that there was not excessive slew (that the signals contained square waves) and that they were the proper voltage (3.3V, 5V, or 6.3V).

2. Pass/Fail Tolerances

The Neuronetrix Headset engineers provided the values for the tolerances, but the method is explained: The circuits all had theoretical values for their outputs and deviations from those values. The resistors and capacitors all had 1% or 5% tolerances

and based on the arrangement of those chips, the tolerances were either constant or additive. Some of the tolerance levels were specifically calculated using tolerances of parts and specifications, such as noise levels and CMRR. Other tests' tolerance levels were calculated but the band which the values fell in where determined experimentally; such as in the frequency response test.

There were several tests designed to validate each Headset. See PS-1487 section 9 for a full description and instructions for use of each test. These tests were integral to ensuring robust, high quality diagnostic devices in the field. The tests are:

- Current Draw
- Noise Test
- Cal Tones Test
- Frequency Response
- Common Mode Rejection Ratio
- Gain linearity
- HCU Function Testing
- Generated Results

Results were generated by a common subVI which included relevant information in the header about the device and test being performed, followed by the test data interpretation. (see PS-1487 section 13 for a copy of Volume Record (VR) 1524.

3. Test Procedure General Overview

Most of the tests are automated with very little action from the user necessary. When a test panel is open, the configuration (See section 6 of PS-1487 for the different configurations) fields are already populated with the default testing conditions (see

Appendix D section 9 for default settings of each VI). If any changes to the configuration need to be made they are done at this time, and then the start button is pressed.

The whole test is performed over the course of a few seconds or minutes and a report is generated. Top level test panels, such as the Master Test Panel, contain automated tests that combine all the other tests, requiring the user to select only those tests which are desired from a list box. Devices are tested primarily in two states, (Luck, 2005) board level testing, and (Fox et al., 1996) finished assembly testing. At the board level the Testset can simulate any of the components of the Headset enabling individual components to be tested independently of each other. For instance, the active electrode strings or the Uberyoke can be tested independent of the HCU and of each other. At the finished assembly level, the Headset can be tested on a test fixture by injecting biosignals into the electrodes simulating a person's brain, while monitoring the communication of the Headset.

4. Analysis Of The Generated Results

Each test produces a set of results, a table or series of values, a graph or chart, and a pass/fail reading for the parameters tested. All raw data was stored in a TDMS file (a data file format by National Instruments) which if necessary can be reconstructed later to reproduce the test. The results, graphs and pass fail parameters are printed to a txt file which is then converted to a PDF file and stored as a part of the Device History Record (DHF). (See a sample report in Appendix D section 13)

5. False Positives Vs. False Negatives

During the design of the tests, and creation of tolerances occasionally a false positive or false negative would occur. While it's undesirable to have these false results, it's best to error on the side of caution. Creating tests that will fail by having a false negative, or rejection, is safer if necessary and results in a retest or further inspection. Having a test that has false positive causes the product to be passed on for further assembly or onto sales, which is undesirable.

6. Noise Test

The Noise Test shorts the active electrodes inputs to ground, effectively removing the electrical influences of anything connected to the electrode, and resulting in any noise that is detected being internal to the Electrode string and/or Uberyoke. Then sampling of all channels occurs as the testset "listens" for any noise. The sampling last for about 25 seconds, which ensures enough time has passed to detect infrequent popcorn noise (See PS-1487 Section 12) coming from bad switch cap filters as well as ensuring that any slow wave (<1 Hz) noise is detected with no less than 2 samples per wave above 0.1 Hz. After the channels have been sampled they are subjected to a variety of processing and testing to make sure that the noise that exist on the channels is below a certain threshold and that there isn't any regularity to it.

7. Cal Tone Test

The Cal tones are pure tone frequencies of 13.8 Hz and 27.6 Hz that are produced in the Uberyoke and travel down the electrode strings and injected into the electrode path at the patient's scalp for the purposes of determining the impedance of the electrodes to the scalp. The reference electrodes emit a low frequency and the other 7 electrodes emit

a higher frequency. The reference signal returns via the regular electrodesThe Caltones' frequencies and amplitudes must be precise in order to properly calculate the impedance via a proprietary equation. This test collects enough samples of data to create an accurate Fourier transform, and then the peaks of the two frequencies are detected and subjected to pass fail examination to determine if they are acceptable.

8. Frequency Response

The Frequency response determines the Headset's bandwidth. The Headset has a Low Pass Filter (LPF) and a High Pass Filter (HPF). The passband region must be within 5% from one Headset to another to ensure accurate results. The test is run by generating a frequency starting at .3 Hz and incrementing the frequency first at 0.1 Hz at a time until 1Hz is achieved, then after that the increment is 1 Hz up to 50 Hz. Beyond 50 Hz the signal to noise ratio is too low as the 33 Hz LPF has reduced the signal below the COGNISION™ Headset's noise level. The test is designed to collect no less than 4 complete cycles per frequency tested to ensure accurate readings. The drawback is that at the frequencies less than 1, the time it takes to capture 4 cycles is longer than the entire test above 1Hz.

9. Common Mode Rejection Ration (CMRR)

Determines the Headset's ability to reject signals that are common to the signal channels and the ground plane. Works identically to the Frequency response test however the signal is injected into the common channel as well as the signal channels and at a greatly amplified value.

10. Crosstalk

The crosstalk test returns information about how much the signal on one channel influences a signal on other channels. This test was performed by generating an 800 μV signal and injecting it into one channel at a time while recording the level of that signal on the other channels. As long as the value on the other channels is below the tolerance the system passes. (See test report for tolerance values Appendix B section 13)

11. Gain Linearity

Returns information about the linearity of the amplifiers. The amplifiers are less linear at very low voltages (voltages less than 5 μV) which unfortunately is not much smaller than the magnitude of the signal the Headset is trying to capture. The test starts at a voltage of 5μV and increments the voltage by 20μV until it reaches the nonlinear region of the DAQ card which is around 700μV. The linearity is calculated by dividing the input by the output for each voltage level. The test is acceptable as long as the value is below .01 for the tested voltages.

12. Power Consumption Test (Current Draw)

When the Headset is first put on the test set and powered up, the current draw is determined by a series of Kelvin circuits. These circuits report the current to the analog inputs on the DAQ card where they are sampled. The current draw in this way can be determined at any time, however a specific test was designed to determine if the Headset has any shorts or opens linked to it's power distribution, by monitoring for abnormalities in its power consumption. The test starts with the system unpowered, then turns the power on and records the value. Then the impedance switches are shorted at which point the power consumption is tested, then the first two steps are done in reverse. If the

current draw is within the acceptable range for each component it is passed (for acceptable ranges see Appendix B section 13 and section 9 under current draw).

13. Time To Complete Testing

A tradeoff between the tests precision and the length of time it takes to perform the test occurs for each of the tests that frequency detection. The more samples collected, the more accurate and precise the test is at detecting the signal. Most of the test use Fourier transforms to move the information from the time domain into the frequency domain. When this happens the number of points of information per frequency is directly correlated with the accuracy of the results. The minimum number of points per frequency in the frequency domain for any test performed with the Testset is 2; however that is only for very low frequencies, most tests collect enough samples in the pass band to ensure a minimum of 4 samples per frequency in the frequency domain.

14. HCU Function Testing

The HCU is a complicated electronic device, with multiple states and functions. Each of the components and firmware must work to their maximum ability for the system to be an effective diagnostic device. Several tests were developed to test each of these HCU components:

15. Field Test

The field test is a proprietary test built into the HCU firmware that tests some internal functionality and is capable of being performed free of the testset. It can be run from the HCU by the user by utilizing a special set of button presses. The field test is able to test the:

Keypad

LCD Screen

Buttons

Audio DAC

Charging Voltage

Uberyoke voltage draw

Audio Output

Audio Attenuator

Bluetooth

The field test generates a report that can be recalled, and stored as part of the Device History Record.

16. HCU Console

The HCU console is the best method for testing the functions of the HCU. It is a comprehensive test suite capable of exercising the functionality of the HCU. The HCU console can perform the Bluetooth discover and pair functions with an HCU; it has the following panels that can interact with these different systems (See PS-1492 section 4 for tests descriptions).

i. Firmware loading

ii. Audio/Audiometry loading

iii. Audio/Audiometry playback (with an audiometer)

iv. Impedance Testing

v. Command Interpretation (Parsing for the different data streams)

vi. Serial number writer (for both Uberyoke and HCU)

vii. Additional testing configurations and detailed information about performing each type of test is presented in PS-1487 of appendix B in sections 4, 7, 9, and 10 with configurations in section 6.

V. RESULTS & DISCUSSION

Once the Testset and software was completed, Headsets were tested on the Testsets and standardized reports were automatically generated at the completion of each test. The automated test suite (the LabVIEW test VIs) took 11.5 minutes to complete all tests on a headset. Two Testsets were used to test one headset for statistical analysis. Sample data was utilized from the FZ channel (a point referring to the electrode location on the head along the central axis near the frontal lobe) (see FIGURE 13) to perform statistical analysis. This channel and test were chosen because they are the most sensitive to failure of any component in the headset. The wire path is the longest, and it is sampled first giving it less settling time than the other channels.

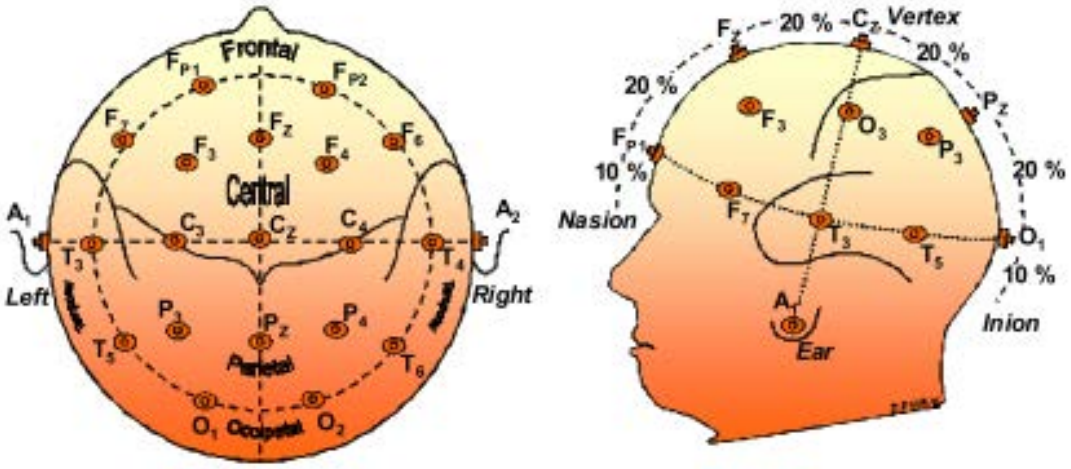


FIGURE 13 : 10-20 International System Of Electrode Placement The Channels Used By The CS System Are : FZ, CZ, PZ, F4, P4, F3, P3, And Dual Mastoid References

A complete test report is presented in PS-1487 section 13 (appendix B), with a detailed description of the parameters and interpretations of the different tests presented in PS-1487 section 11. Aberrant tests results of significance are displayed in PS-1487 section 12. There are many tools that have been developed to probe the Headset, however, there are a few automated test that are capable of producing a text based test report with associated image files of the graphs produced. While the tests are described in detail as is the results in the PS-1487, a brief description of each of the test results is below. The tests and results are all channel by channel. Results are given with a legend with reference ranges for acceptable values. The electrodes are all named by the EEG industry standard of the 10:20 system (Niedermeyer & Schomer, 2011).

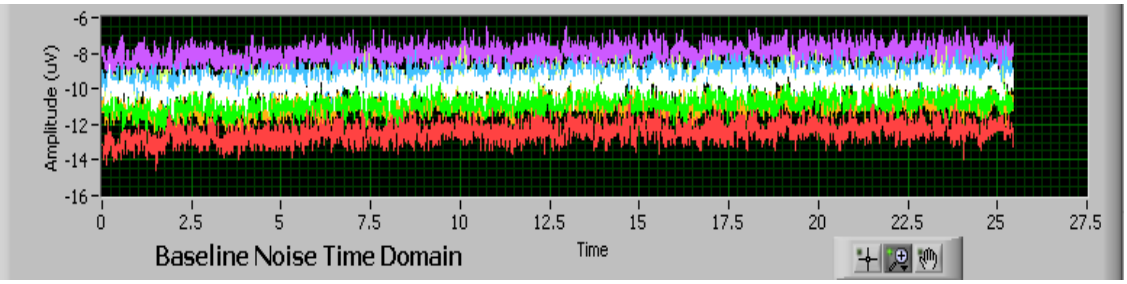


FIGURE 14 : Baseline Noise Time Domain Graph, Shows The Measurement Of Internal Noise Occurring In The Uberyoke. Notice That The Results Signals Change Less Than 5 V Pk-Pk

A. The Noise and Calibration Tones (Cal tones) test

This tests the internal noise values, and the Cal Tones. The noise test (see

FIGURE 14 and Table for results) collects data without any input into the electrodes to determine the internal noise of the system. The calibration tones are tones of a calibrated frequency and amplitude (see

FIGURE 15 and Table for results). The frequency and amplitude must fall within a narrow range. This test takes duration of 1:46 mm:ss to complete on average.

TABLE I

NOISE AND CALTONES TEST RESULTS FOR THE FZ CHANNEL

PASS: 3.051804 µV	Noise Vpk-pk: < 5 µV
PASS: 0.478274 µV	Noise V RMS: < 1 µV
PASS: 13.674458 Hz	Low Cal Frequency: 13.50 - 14.50 Hz
PASS: 32.551223 µV	Low Cal Power: 31.5 - 33.5 dB µV
PASS: 27.349418 Hz	High Cal Frequency: 27.00 - 28.00 Hz
PASS: 32.624808 µV	High Cal Power: 31.5 - 33.5 dB µV

The noise test is important for detecting single "pops" in the data sample. Pops amongst other common kinds of noises are single peaks of relatively high frequency. These are the most common rejection criteria for a headset as the switch cap filter is not manufactured to a tight enough tolerance. As a result even after a "binning" process where post purchased testing eliminates all but a few of the unacceptable switch cap filters a few are not able to pass the noise test. Unfortunately in order to catch units that have unacceptable switch cap filters that generate pop corn noise, tolerances end up being tighter than the variation in the amplifiers during the warm up phase, resulting in the test taking extra time. The Cal tones which are generated by a microcontroller has only failed if the commands are not being received by the yoke's microprocessor or there is an open

or short in the circuit. Solder bridges or poorly soldered vias are the most common cause of this failure. Any amount of noise that is underneath the fail level should result in uniformity for the data collected from patients by the headset.

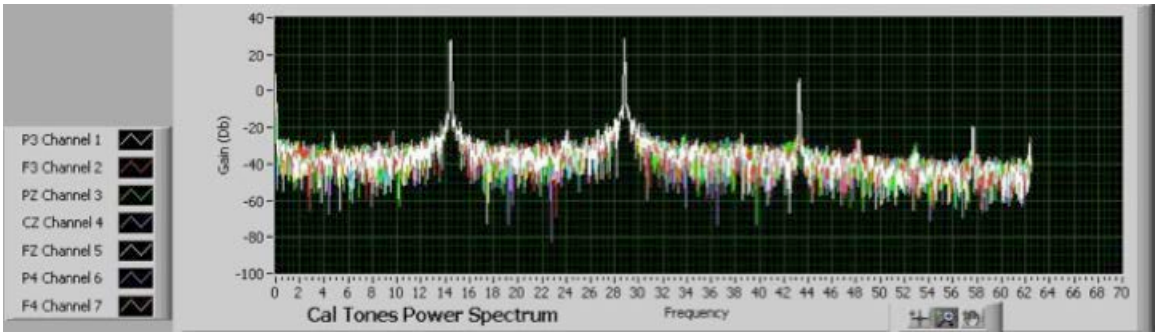


FIGURE 15 : Cal Tones Power Spectrum (Notice The Peaks At 14 And 28 Hz)

B. Frequency Response Test Results

TABLE II

THE SAMPLE RESULTS GENERATED FROM THE FREQUENCY RESPONSE TEST FOR THE FZ CHANNEL.

FZ / 1	Electrode / Channel
PASS: data within tolerance	Max Deviation: < 0.45 dB @ 0.3-39 Hz
PASS: data within tolerance	Max Deviation: < 2 dB @ 40-50 Hz
PASS: -2.69	Gain @ 33 Hz: -3.50 < x < -2.50 dB
PASS: 0.04	Gain @ 10 Hz: -0.50 < x < 0.05 dB
PASS: -3.17	Gain @ 0.4 Hz: -4.25 < x < -3.25 dB
PASS: 0.7674	Variance 1-20 Hz : < 1 dB

There is an optimal value for each parameter. This test takes 3:09 mm:ss to complete on average. The max deviation parameter ensures that the gain values for each frequency is within a certain range of the "expected output." This parameter fails if the amplifiers are not set correctly, either a resistor is swapped with the wrong value or the amplifiers are not powered correctly was the only cause for this to fail and resulted in values with a deviation greater than the 0.45 for the pass band (See Table and left for results).

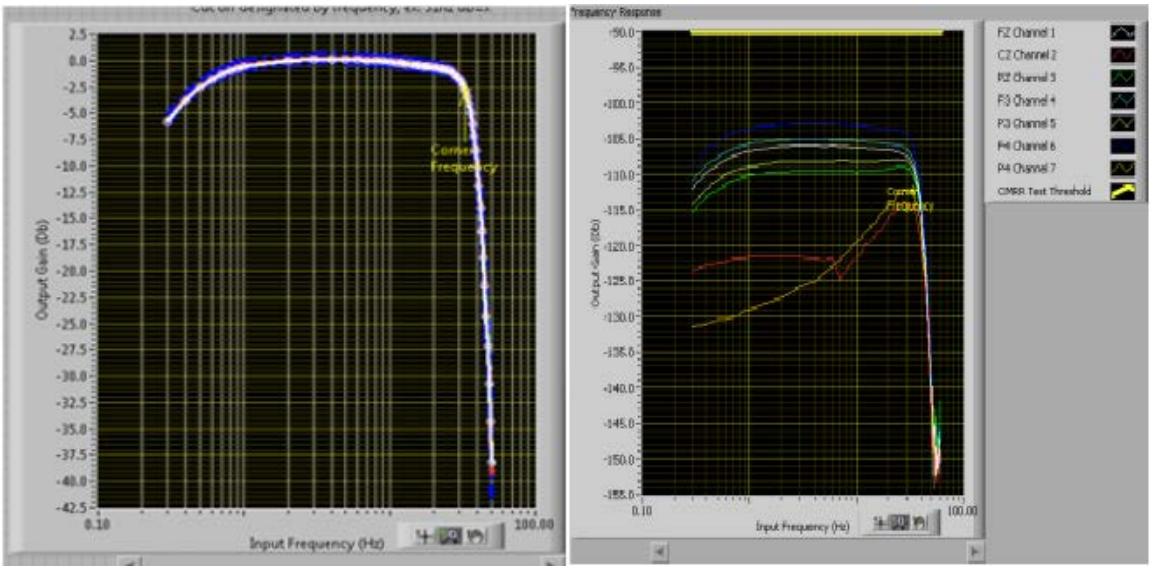


FIGURE 16 : (Left) Frequency Response Curve, Notice The 3 Sections: High Pass From 0.3 To 1 Hz, Bandpass From 1 To 33 Hz, And Low Pass From 33 To 60 Hz (Right) CMRR Output Image. All Outputs Are Below 90 Db, With The Filters Rejecting The 60 Hz Region Down To 150 Db.

C. CMRR RESULTS

TABLE III

SAMPLE RESULTS GENERATED FROM THE CMRR TEST FOR THE FZ CHANNEL.

FZ / 1	Electrode / Channel
PASS: -95.41	Min Attenuation: < 90 dB
PASS: -142.98	CMRR @ 60 HZ: <100 dB
PASS: -134.87	CMRR @ 50 HZ: < 100 dB

The CMRR (See and TABLE III) is the amount of noise rejected when the signal is common to all channels. The CMRR on average test takes 3:29 mm:ss to complete. The lower the signal captured the better the results. The minimum attenuation is 90 db. The different channels varied from unit to unit by a wide margin however they were all under the 90 db mark. The only failure of this circuit occurred when a polarized capacitor was not being checked for its polarity.

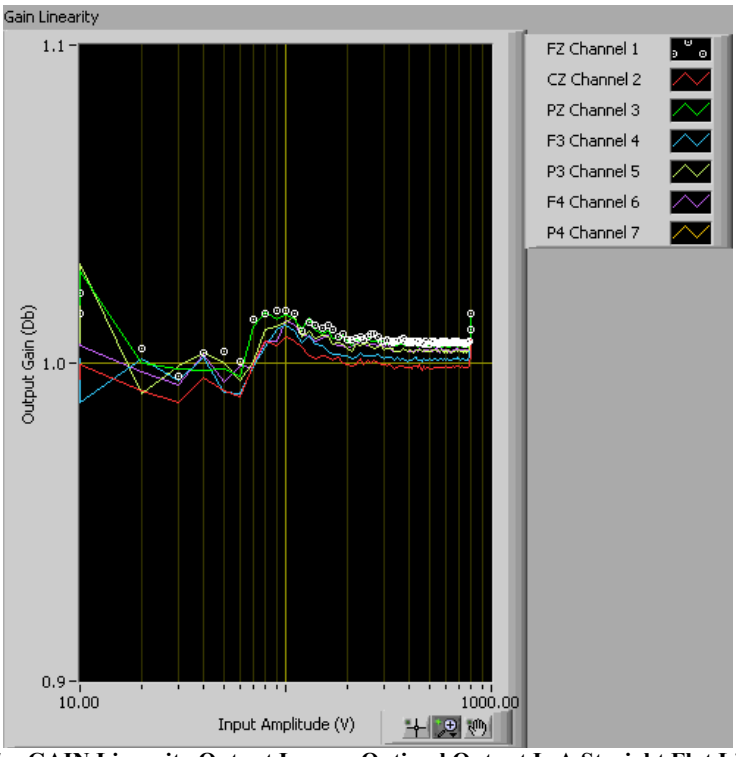


FIGURE 17 : GAIN Linearity Output Image. Optimal Output Is A Straight Flat Line With X = 1.0

D. GAIN RESULTS

TABLE IV

SAMPLE RESULT GENERATED FROM THE GAIN LINEARITY TEST FOR THE FZ CHANNEL.

FZ / 1	Electrode / Channel
PASS: 0.025	Maximum deviation from linearity : < 0.1

This gain lineary test takes 3:37 mm:ss on average. The gain channels gain ratio stayed between 1.1 and 0.09 for the duration of the test, showing that the amplifier had a linear relationship with the signal input and the amplifier output. The maximum deviation from linearity was 0.025. This test only fails when the amplifier is non linear, usually this is caused by interference since there hasn't been any faulty amplifiers tested. A Headset was repeatedly tested on one Testset and the data was found to support the

hypothesis that there was no significant difference in the values collected for the noise test on channel FZ with a confidence interval of 95%. This conclusion was achieved by running a 1 sample T test on the headset using Testset 1.

TABLE V

DATASET FROM TESTSET 1

Pk/Pk noise (µV)	RMS noise (µV)	low tone (HZ)	High tone (V)	high tone (HZ)	high tone (V)
3.05180	0.473222	13.6719	32.6013	27.3438	32.5951
3.32924	0.503080	13.6719	32.5904	27.3438	32.5797
3.32924	0.471722	13.6719	32.5969	27.3438	32.5850
3.15180	0.473683	13.6719	32.5920	27.3437	32.5947
3.32924	0.462220	13.6719	32.5914	27.3438	32.5894
3.19052	0.479449	13.6719	32.5995	27.3438	32.5940
3.05180	0.464851	13.6719	32.5924	27.3438	32.5956
3.32924	0.488411	13.6719	32.5882	27.3438	32.5955
3.16796	0.480544	13.6719	32.5908	27.3438	32.5935
3.32924	0.492288	13.6719	32.5987	27.3438	32.6001

TABLE VI

OUTPUT FROM MINI TAB FOR T TEST ON DATASET 1

Variable	N	Mean	StDev	SE	95% CI	
C1	10	3.2460	0.1491	0.0472	(3.1393	3.3527)
C2	10	0.4862	0.0366	0.0116	(0.4600	0.5123)
C3	10	13.6719	0.0000	0.0000	(13.6719	13.6719)
C4	10	32.5942	0.0045	0.0014	(32.5909	32.5974)
C5	10	27.3438	0.0000	0.0000	(27.3437	27.3438)
C6	10	32.5923	0.0060	0.0019	(32.5880	32.5965)

All data fell within the 95% confidence interval. The Cal tones were shown to be read very precisely as they did not differ into the hundredths place for any of the values collected. These values show that when a test is repeatedly performed on a headset, that headset's values all fall within a narrow enough band to not yield a statistically significant difference. The T-test performed on the results show that with at least 95% confidence, these values did not different significantly. In fact for the frequencies of the

low and high tone, the values did not differ at all within the precision being captured. For the purposes of collecting ERPs these values show that there is no temporal change in the unit that would cause significant differences in the data collected. Additionally this headset was tested on the other testset and a comparison of the two Testsets was made.

The hypothesis that the Testsets were independent of the data collected was supported with a 95% confidence interval.

TABLE VII

DATASET FROM TESTSET 2

Pk/Pk noise (μV)	RMS noise (μV)	low tone (HZ)	low tone (V)	high tone (HZ)	high tone (V)
3.34761	0.493075	13.6719	32.5904	27.3438	32.5797
3.32924	0.485670	13.6719	32.5914	27.3438	32.5894
3.32824	0.497560	13.6719	32.5987	27.3437	32.6001
3.35430	0.465432	13.6719	32.5969	27.3438	32.5850
3.32924	0.475640	13.6719	32.5883	27.3438	32.5956
3.17564	0.486575	13.6719	32.5920	27.3438	32.5941
3.08180	0.485750	13.6719	32.5948	27.3438	32.5951
3.19052	0.485644	13.6719	32.5995	27.3438	32.5939
3.05180	0.467565	13.6719	32.5924	27.3438	32.5956
3.16796	0.496456	13.6719	32.5908	27.3438	32.5939

The values from tables 6 and 7 show that when a test is repeatedly performed on a headset, that headset's values all fall within a narrow enough band to not yield a statistically significant difference. The T test performed on the results show that with at least 95% confidence, these values did not different significantly. In fact for the frequencies of the low and high tone, the values did not differ at all within the precision being captured. For the purposes of collecting ERPs these values show that there is no temporal change in the unit that would cause significant differences in the data collected.

TABLE VIII

PAIRED T TEST FOR DATASET 1 AND 2 FROM TESTSET 1 AND 2

	N	Mean	StDev	Mean
FZ1	10	3.2260	0.1174	0.0371
FZ2	10	3.2356	0.1157	0.0366
Difference	10	-0.0096	0.1443	0.0456

Paired T for FZ1 - FZ2 95% CI for mean difference: (-0.1129, 0.0936) T-Test of mean difference = 0 (vs. not = 0): T-Value = -0.21 P-Value = 0.838

After showing that the Headsets can be repeatedly tested on an individual headset without a statistically significant difference between one test and the next it remained to show that there was no significant difference between testing on the two different Testsets. The paired T test on the two data sets shows that there is not a statistically significant difference between testing on Testset 1 or Testset 2. Either Testset can be used and there will not be a different outcome in the results for a particular headset. This supports the hypothesis that there is no difference between the two Testsets with regards to the differences in voltages levels in nano volts.

Similar analysis was done on the gain values at different frequencies for the frequency response test. The frequency response test was performed at a similar voltage of what is expected of the bio signals generated from the brain, 50 μV.

TABLE IX

FREQUENCY RESPONSE DATA FROM TESTSET 1

57.13	59.89	62.8177
57.22	59.94	56.5200
57.18	59.95	56.5100
57.22	59.96	56.4500
57.20	59.89	61.7500
57.19	59.94	56.5000
57.18	59.90	56.3800
57.22	59.94	56.4500

TABLE X

ONE-SAMPLE T: 0.2-0.9, 1-33, 33-50 FROM TABLE 9 FOR TESTSET 1

Variable	N	Mean	StDev	SE Mean	95% CI	
0.2-0.9	8	57.1937	0.0320	0.0113	(57.1670	57.2205)
1-33	8	59.9262	0.0283	0.0100	(59.8026	59.9510)
33-50	8	57.922	2.708	0.957	(55.659	62.186)

The values from Tables 9 and 10 show that when a test is repeatedly performed on a headset, that headset's values all fall within a narrow enough band to not yield a statistically significant difference. The T test performed on the results show that with at least 95% confidence, these values did not different significantly. For the purposes of collecting ERPs these values show that there is no temporal change in the unit that would cause significant differences in the data collected.

TABLE XI

FREQUENCY RESPONSE DATA FROM TESTSET 2

57.16	59.94	60.8177
57.24	59.89	57.8900
57.17	59.95	55.4900
57.20	59.93	56.4600
57.19	59.89	61.6500
57.19	59.94	57.5000
57.24	59.90	58.5600
57.22	59.88	57.2700

TABLE XII

ONE-SAMPLE T: 0.2-0.9, 1-33, 33-50 – FROM TABLE 11 FOR TESTSET 2

Variable	N	Mean	StDev	SE Mean	95% CI	
0.2-0.9	8	57.2013	0.0300	0.0106	(57.1562	57.2263)
1-33	8	59.9150	0.0278	0.0098	(59.8918	59.9382)
33-50	8	58.205	2.094	0.740	(56.454	59.956)
Variable	N	Mean	StDev	SE Mean	95% CI	
0.2-0.9	8	57.2013	0.0300	0.0106	(57.1562	57.2263)
1-33	8	59.9150	0.0278	0.0098	(59.8918	59.9382)
33-50	8	58.205	2.094	0.740	(56.454	59.956)

The values from Table 11 and 12 show that when a test is repeatedly performed on a headset, that headset's values all fall within a narrow enough band to not yield a statistically significant difference. The T test performed on the results show that with at least 95% confidence, these values did not different significantly. In fact for the frequencies of the low and high tone, the values did not differ at all within the precision being captured. For the purposes of collecting ERPs these values show that there is no temporal change in the unit that would cause significant differences in the data collected.

TABLE XIII

TWO-SAMPLE T-TEST AND CI: 0.2-0.9, T2 0.2-0.9

	N	Mean	StDev	SE Mean
0.2-0.9	8	57.2013	0.0300	0.011
0.2-0.9	8	57.1925	0.0306	0.011

Two-sample T for 0.2-0.9 vs t2 0.2-0.9

Difference = mu (0.2-0.9) - mu (t2 0.2-0.9)

Estimate for difference: 0.0088

95% CI for difference: (-0.0240, 0.0415)

T-Test of difference = 0 (vs not =): T-Value = 0.58 P-Value = 0.573 DF = 13

This supports the hypothesis that there is no difference between the two Testsets with regards to the differences in voltages levels in millivolts, and that the amplified values from the headsets and input to the Testsets do not have any statistically significant differences.

The results and statistical analysis from the noise test and the frequency response test concur with each other and support the established hypotheses.

VI. DISCUSSION

The benefits of using LabVIEW to control and automate the Testset instead of other methods are numerous. The interfaces are already standardized; buttons and displays are drag and drop. A control panel can be started and finished in an hour. According to a study published by National Instruments (Goodin, Squires, & Starr, 1978) the company was able to save 60 percent of their initial investment and floor space. These compact automated units that are able to perform all the task from a single test fixture reducing the afmount of space and time. Once one of the printed circuit boards are mounted on the test fixture, the test can run freely; there is no time lost due to removing the printed circuit board and placing it on a second or third test fixture, likewise there isn't any time lost to changing settings in between test. Ideally, 3 or 4 Testsets would be in operation simultaneously, and one technician would operate them in order, by setting them up and starting the test before moving to the next one. Thereby keeping a constant cycle of mounting, starting tests and un-mounting the boards.

Initially the system was designed to use the DAQ card's analog channels to record the playback from the audio components, however, it turned out the dynamic range of the analog inputs were not adequate/sufficient to support audio. Audio usually has a small step size in the μV, a 12 bit input with a dynamic range of ±5V results in a step size of 2.44 volts. This is 1000 times the necessary step size as the smallest detectable amplitude was the equivalent of 60 db on a pair of conventional headphones. In a redesign of the Testboard, an audio DAC could have been used, but a conventional USB audio card was

used instead which had inputs that had a suitable dynamic range of 24 bits and ± 3V resulting in a step size of around 300 nano volts.

During testing some electrode strings exhibited some irregular CMRR's that turned out to be correlated with some polarized capacitors being placed on the board backwards. Not all of the capacitors when reversed resulted in the ability to reject the electrode with the current equipment. In a future model an additional circuit will be added to test whether these capacitors were soldered on in reverse configuration.

Currently, the test protocol requires a visual inspection before the boards can be tested. To identify solder bridges, missing chips, and/or other defects. New inexpensive, easy to automate software by National Instruments called MACHINE VISION allows rapid image comparisons for visual inspection of equipment such as circuit boards. Most tests in the validation protocol will catch anything wrong with the boards, except poorly soldered joints, but there isn't a way to test the presence of the TVS diodes that protect the patients in the instance of some sort of electric discharge.

Another huge change would be to change the method of signal generation. The testset has a 128 point signal that can be repeated at up to 60 Hz, which can be increased at the cost of the number of points. (2000 Hz is attainable with only around 20 or so data points). A more advanced signal generator would be able to simulate a signwave for instance with a high number of points without sacrificing bandwidth. Additionally, and more importantly, a different signal generator could produce multiple frequencies simultaneously allowing tests such as CMRR, frequency response, and cross talk to be done in seconds instead of minutes, thereby increasing throughput, productivity, and reducing the cost of testing.

This type of design is remarkable in that it was done by the work of one engineer, in the short amount of time. Only recently have computers reached a speed fast enough, and the G programming language intuitive enough that this has become a possibility. From start of the design to the fabrication of the boards, the entire process was controlled and designed on the computer. The productivity increase in industry as a result of this type of ability should lead to cheaper quality control systems, and more of them available to small businesses and custom manufacturing.

Medical devices have a particularly inelastic demand for quality goods, with very little margin for faulty equipment. Risk management is very high on this list because not only does the dollar drive the bottom line (cost of lawsuits for defective pacemakers vs. the cost to improve the fault detection) but there are ethical and moral considerations that decrease obsolesce and failures. A diagnostic device that serves as early warning for disease or a heart pump that literally has a life hanging in the balance will most certainly cause pain and suffering if the device fails or behaves aberrantly. So the development of fully automated and inexpensive test systems is a major boon to decreasing the cost of medical care. The advantage is that as more of these systems are employed economies of scale will occur, and other industries may be able to take advantage of the testing platforms for things that may have had a less robust vetting process in the past.

VII. CONCLUSION

The Headset was developed for more effectively collecting ERP and EEG data for the purposes of diagnosing cognitive disorders. The headset is a technologically complex machine that requires testing to comply with regulatory rules. To test and validate this medical device two test were developed. The Testset is capable of testing the entire suite of Headset functions. It meets all specifications, and is automated. The hypothesis of this thesis is supported that a Testset can reliably test a Headset without statistically significant variation in the data. The hypothesis is supported that the two Testsets created have a high probability of not yielding different results from one another. The software is able to drive the hardware appropriately and statistical analysis shows that the two Testsets in use produce data that is reliable and consistent with each other.

VIII. SUGGESTIONS

The suggestions for this project revolve around the single decision to utilize a small third party (non National Instruments) brand of data acquisition card. Labjack, while a very robust DAQ had many issues that would have been resolved by a more equipped card, particularly if it wasn't connected via Ethernet or USB, but rather a direct connection to the mother board. The difference in price for the unit was 10 fold, 5000 vs. 500. However, several extra 10k's where spent as a result of trying to get around the issues that came with an in adequate card.

Appendix A – Specification Documents

MICROCHIP

MCP23008/MCP23S08

8-Bit I/O Expander with Serial Interface

Features

- 8-bit remote bidirectional I/O port
  - I/O pins default to input
- High-speed I^2C™ interface (**MCP23008**)
  - 100 kHz
  - 400 kHz
  - 1.7 MHz
- High-speed SPI™ interface (**MCP23S08**)
  - 10 MHz
- Hardware address pins
  - Three for the MCP23008 to allow up to eight devices on the bus
  - Two for the MCP23S08 to allow up to four devices using the same chip-select
- Configurable interrupt output pin
  - Configurable as active-high, active-low or open-drain
- Configurable interrupt source
  - Interrupt-on-change from configured defaults or pin change
- Polarity Inversion register to configure the polarity of the input port data
- External reset input
- Low standby current: 1 µA (max.)
- Operating voltage:
  - 1.8V to 5.5V @ -40°C to +85°C (I-Temp)
  - 2.7V to 5.5V @ -40°C to +85°C (I-Temp)
  - 4.5V to 5.5V @ -40°C to +125°C (E-Temp)

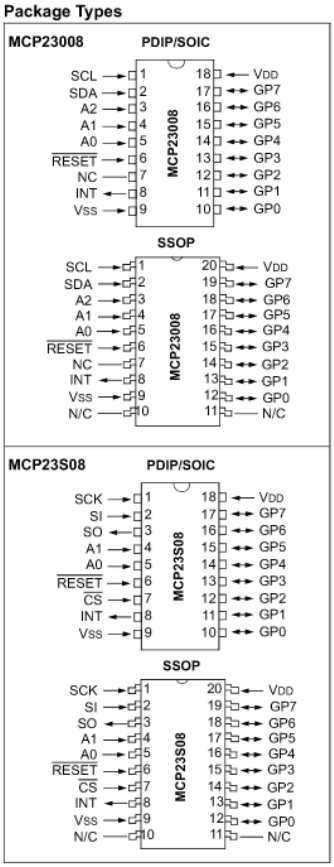
Packages

18-pin PDIP (300 mil)

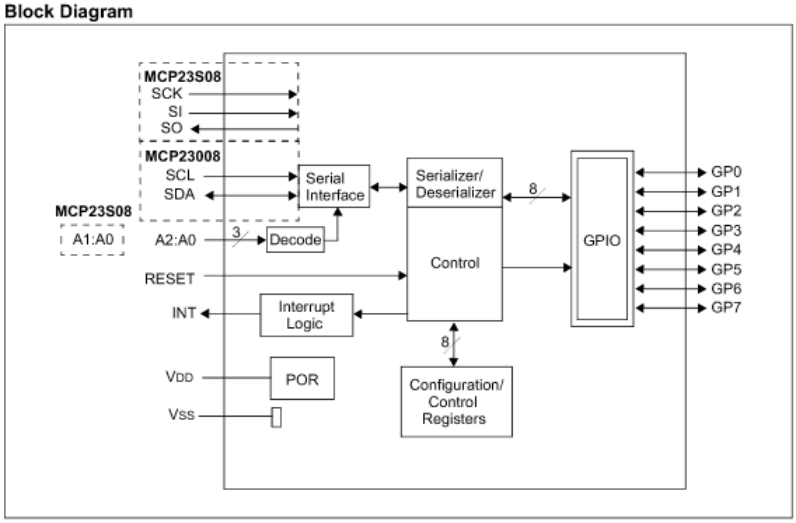
18-pin SOIC (300 mil)

20-pin SSOP

Package Types



Block Diagram



1.0 DEVICE OVERVIEW

The MCP23X08 device provides 8-bit, general purpose, parallel I/O expansion for I^2C bus or SPI applications. The two devices differ in the number of hardware address pins and the serial interface:

- MCP23008 – I^2C interface; three address pins
- MCP23S08 – SPI interface; two address pins

The MCP23X08 consists of multiple 8-bit configuration registers for input, output and polarity selection. The system master can enable the I/Os as either inputs or outputs by writing the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The interrupt output can be configured to activate under two conditions (mutually exclusive):

1. When any input state differs from its corresponding input port register state. This is used to indicate to the system master that an input state has changed.
2. When an input state differs from a preconfigured register value (DEFVAL register).

The Interrupt Capture register captures port values at the time of the interrupt, thereby saving the condition that caused the interrupt.

The Power-on Reset (POR) sets the registers to their default values and initializes the device state machine.

The hardware address pins are used to determine the device address.

1.1 Pin Descriptions

TABLE 1-1: PINOUT DESCRIPTION

Pin Name	PDIP/SOIC	SSOP	Pin Type	Function
SCL/SCK	1	1	I	Serial clock input.
SDA/SI	2	2	I/O	Serial data I/O (**MCP23008**)/Serial data input (**MCP23S08**).
A2/SO	3	3	I/O	Hardware address input (**MCP23008**)/Serial data output (**MCP23S08**). A2 must be biased externally.
A1	4	4	I	Hardware address input. Must be biased externally.
A0	5	5	I	Hardware address input. Must be biased externally.
$\overline{\text{RESET}}$	6	6	I	External reset input
NC/$\overline{\text{CS}}$	7	7	I	No connect (**MCP23008**)/External chip select input (**MCP23S08**).
INT	8	8	O	Interrupt output. Can be configured for active-high, active-low or open-drain.
VSS	9	9	P	Ground.
GP0	10	12	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP1	11	13	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP2	12	14	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP3	13	15	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP4	14	16	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP5	15	17	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP6	16	18	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP7	17	19	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
VDD	18	20	P	Power.
N/C		10, 11		

1.2 Power-on Reset (POR)

The on-chip POR circuit holds the device in reset until VDD has reached a high enough voltage to deactivate the POR circuit (i.e., release the device from reset). The maximum VDD rise time is specified in **Section 2.0 "Electrical Characteristics"**.

When the device exits the POR condition (releases reset), device operating parameters (i.e., voltage, temperature, serial bus frequency, etc.) must be met to ensure proper operation.

1.3 Serial Interface

This block handles the functionality of the I^2C (MCP23008) or SPI (MCP23S08) interface protocol. The MCP23X08 contains eleven registers that can be addressed through the serial interface block (Table 1-2):

TABLE 1-2: REGISTER ADDRESSES

Address	Access to:
00h	IODIR
01h	IPOL
02h	GPINTEN
03h	DEFVAL
04h	INTCON
05h	IOCON
06h	GPPU
07h	INTF
08h	INTCAP (Read-only)
09h	GPIO
0Ah	OLAT

1.3.1 SEQUENTIAL OPERATION BIT

The Sequential Operation (SEQOP) bit (IOCON register) controls the operation of the address pointer. The address pointer can either be enabled (default) to allow the address pointer to increment automatically after each data transfer, or it can be disabled.

When operating in **Sequential mode** (IOCON.SEQOP = 0), the address pointer automatically increments to the next address after each byte is clocked.

When operating in **Byte mode** (IOCON.SEQOP = 1), the MCP23X08 does not increment its address counter after each byte during the data transfer. This gives the ability to continually read the same address by providing extra clocks (without additional control bytes). This is useful for polling the GPIO register for data changes.

1.3.2 I^2C™ INTERFACE

1.3.2.1 I^2C Write Operation

The I^2C Write operation includes the control byte and register address sequence, as shown in the bottom of Figure 1-1. This sequence is followed by eight bits of data from the master and an Acknowledge (ACK) from the MCP23008. The operation is ended with a STOP or RESTART condition being generated by the master.

Data is written to the MCP23008 after every byte transfer. If a STOP or RESTART condition is generated during a data transfer, the data will not be written to the MCP23008.

Byte writes and sequential writes are both supported by the MCP23008. The MCP23008 increments its address counter after each ACK during the data transfer.

1.3.2.2 I^2C Read Operation

The I^2C Read operation includes the control byte sequence, as shown in the bottom of Figure 1-1. This sequence is followed by another control byte (including the START condition and ACK) with the R/W bit equal to a logic 1 (R/W = 1). The MCP23008 then transmits the data contained in the addressed register. The sequence is ended with the master generating a STOP or RESTART condition.

1.3.2.3 I^2C Sequential Write/Read

For sequential operations (Write or Read), instead of transmitting a STOP or RESTART condition after the data transfer, the master clocks the next byte pointed to by the address pointer (see **Section 1.3.1 "Sequential Operation Bit"** for details regarding sequential operation control).

The sequence ends with the master sending a STOP or RESTART condition.

The MCP23008 address pointer will roll over to address zero after reaching the last register address.

Refer to Figure 1-1.

1.3.3 SPI™ INTERFACE

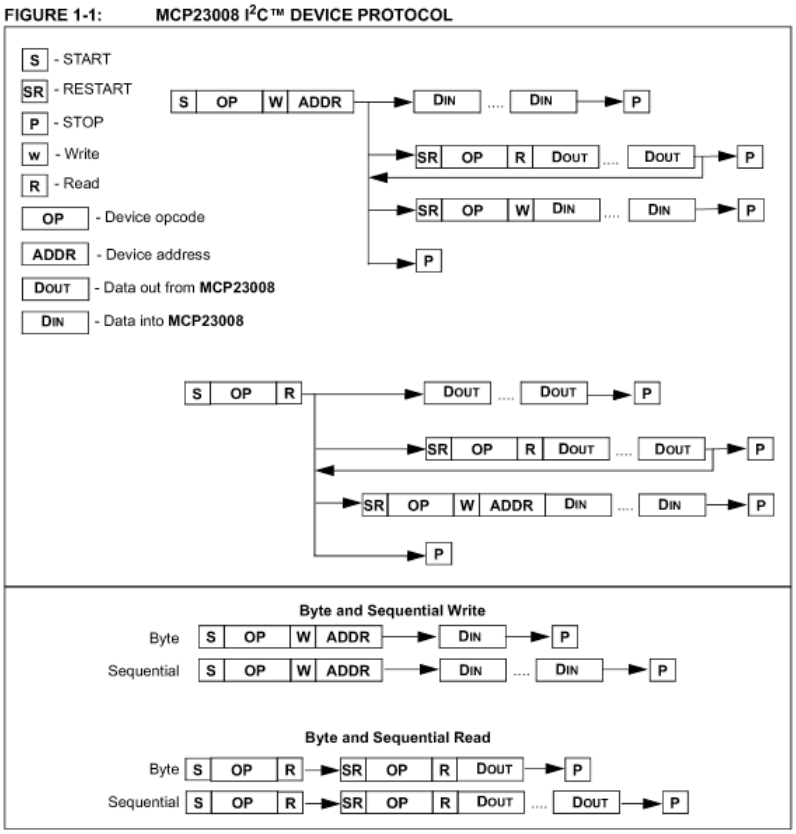
1.3.3.1 SPI Write Operation

The SPI Write operation is started by lowering $\overline{CS}$. The Write command (slave address with R/W bit cleared) is then clocked into the device. The opcode is followed by an address and at least one data byte.

1.3.3.2 SPI Read Operation

The SPI Read operation is started by lowering $\overline{CS}$. The SPI read command (slave address with R/W bit set) is then clocked into the device. The opcode is followed by an address, with at least one data byte being clocked out of the device.

FIGURE 1-1: MCP23008 I²C™ DEVICE PROTOCOL



1.3.3.3 SPI Sequential Write/Read

For sequential operations, instead of deselecting the device by raising $\overline{CS}$, the master clocks the next byte pointed to by the address pointer.

The sequence ends by the raising of $\overline{CS}$.

The MCP23S08 address pointer will roll over to address zero after reaching the last register address.

1.4 Hardware Address Decoder

The hardware address pins are used to determine the device address. To address a device, the corresponding address bits in the control byte must match the pin state.

- MCP23008 has address pins A2, A1 and A0.
- MCP23S08 has address pins A1 and A0.

The pins must be biased externally.

1.4.1 ADDRESSING I²C DEVICES (MCP23008)

The MCP23008 is a slave I²C device that supports 7-bit slave addressing, with the read/write bit filling out the control byte. The slave address contains four fixed bits and three user-defined hardware address bits (pins A2, A1 and A0). Figure 1-2 shows the control byte format.

1.4.2 ADDRESSING SPI DEVICES (MCP23S08)

The MCP23S08 is a slave SPI device. The slave address contains five fixed bits and two user-defined hardware address bits (pins A1 and A0), with the read/write bit filling out the control byte. Figure 1-3 shows the control byte format.

FIGURE 1-2: I²C™ CONTROL BYTE FORMAT

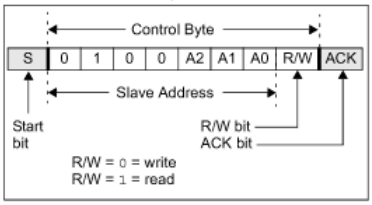


FIGURE 1-3: SPI™ CONTROL BYTE FORMAT

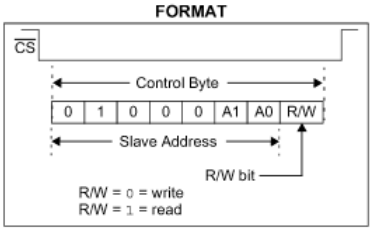


FIGURE 1-4: I²C™ ADDRESSING REGISTERS

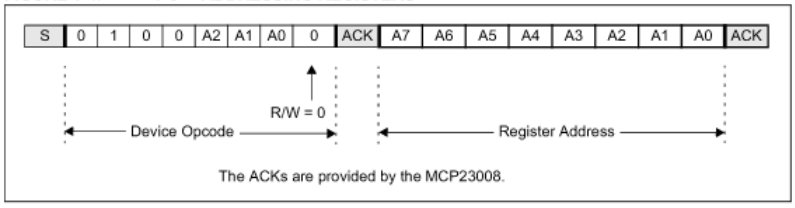
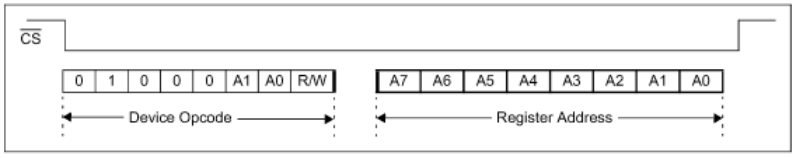


FIGURE 1-5: SPI™ ADDRESSING REGISTERS



1.5 GPIO Port

The GPIO module contains the data port (GPIO), internal pull up resistors and the Output Latches (OLAT).

Reading the GPIO register reads the value on the port. Reading the OLAT register only reads the OLAT, not the actual value on the port.

Writing to the GPIO register actually causes a write to the OLAT. Writing to the OLAT register forces the associated output drivers to drive to the level in OLAT. Pins configured as inputs turn off the associated output driver and put it in high-impedance.

1.6 Configuration and Control Registers

The Configuration and Control blocks contain the registers as shown in Table 1-3.

TABLE 1-3: CONFIGURATION AND CONTROL REGISTERS

Register Name	Address (hex)	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	POR/RST value
IODIR	00	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	1111 1111
IPOL	01	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000 0000
GPINTEN	02	GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0	0000 0000
DEFVAL	03	DEF7	DEF6	DEF5	DEF4	DEF3	DEF2	DEF1	DEF0	0000 0000
INTCON	04	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	0000 0000
IOCON	05	—	—	SREAD	DISSLW	HAEN *	ODR	INTPOL	—	--00 000-
GPPU	06	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0000 0000
INTF	07	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INTO	0000 0000
INTCAP	08	ICP7	ICP6	ICP5	ICP4	ICP3	ICP2	ICP1	ICP0	0000 0000
GPIO	09	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
OLAT	0A	OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0	0000 0000

* Not used on the MCP23008.

1.6.1 I/O DIRECTION (IODIR) REGISTER

Controls the direction of the data I/O.

When a bit is set, the corresponding pin becomes an input. When a bit is clear, the corresponding pin becomes an output.

REGISTER 1-1: IODIR – I/O DIRECTION REGISTER (ADDR 0x00)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
bit 7							bit 0

bit 7-0 **IO7:IO0:** These bits control the direction of data I/O <7:0>.
1 = Pin is configured as an input.
0 = Pin is configured as an output.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

1.6.2 INPUT POLARITY (IPOL) REGISTER

The IPOL register allows the user to configure the polarity on the corresponding GPIO port bits.

If a bit is set, the corresponding GPIO register bit will reflect the inverted value on the pin.

REGISTER 1-2: IPOL – INPUT POLARITY PORT REGISTER (ADDR 0x01)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
bit 7							bit 0

bit 7-0 **IP7:IP0:** These bits control the polarity inversion of the input pins <7:0>.
1 = GPIO register bit will reflect the opposite logic state of the input pin.
0 = GPIO register bit will reflect the same logic state of the input pin.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

1.6.3 INTERRUPT-ON-CHANGE CONTROL (GPINTEN) REGISTER

The GPINTEN register controls the interrupt-on-change feature for each pin.

If a bit is set, the corresponding pin is enabled for interrupt-on-change. The DEFVAL and INTCON registers must also be configured if any pins are enabled for interrupt-on-change.

REGISTER 1-3: GPINTEN – INTERRUPT-ON-CHANGE PINS (ADDR 0x02)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0
bit 7							bit 0

bit 7-0 **GPINT7:GPINT0:** General purpose I/O interrupt-on-change bits <7:0>.
1 = Enable GPIO input pin for interrupt-on-change event.
0 = Disable GPIO input pin for interrupt-on-change event.

Refer to INTCON and GPINTEN.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

1.6.4 DEFAULT COMPARE (DEFVAL) REGISTER FOR INTERRUPT-ON-CHANGE

The default comparison value is configured in the DEFVAL register. If enabled (via GPINTEN and INTCON) to compare against the DEFVAL register, an opposite value on the associated pin will cause an interrupt to occur.

REGISTER 1-4: DEFVAL – DEFAULT VALUE REGISTER (ADDR 0x03)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DEF7	DEF6	DEF5	DEF4	DEF3	DEF2	DEF1	DEF0
bit 7							bit 0

bit 7-0 **DEF7:DEF0:** These bits set the compare value for pins configured for interrupt-on-change from defaults <7:0>. Refer to INTCON.
If the associated pin level is the opposite from the register bit, an interrupt occurs.

Refer to INTCON and GPINTEN.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

1.6.5 INTERRUPT CONTROL (INTCON) REGISTER

The INTCON register controls how the associated pin value is compared for the interrupt-on-change feature. If a bit is set, the corresponding I/O pin is compared against the associated bit in the DEFVAL register. If a bit value is clear, the corresponding I/O pin is compared against the previous value.

REGISTER 1-5: INTCON – INTERRUPT-ON-CHANGE CONTROL REGISTER (ADDR 0x04)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0
bit 7							bit 0

bit 7-0 **IOC7:IOC0:** These bits control how the associated pin value is compared for interrupt-on-change <7:0>.

1 = Controls how the associated pin value is compared for interrupt-on-change.
0 = Pin value is compared against the previous pin value.

Refer to INTCON and GPINTEN.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

1.6.6 CONFIGURATION (IOCON) REGISTER

The IOCON register contains several bits for configuring the device:

- The Sequential Operation (SEQOP) controls the incrementing function of the address pointer. If the address pointer is disabled, the address pointer does not automatically increment after each byte is clocked during a serial transfer. This feature is useful when it is desired to continuously poll (read) or modify (write) a register.
- The Slew Rate (DISSLW) bit controls the slew rate function on the SDA pin. If enabled, the SDA slew rate will be controlled when driving from a high to a low.
- The Hardware Address Enable (HAEN) control bit enables/disables the hardware address pins (A2, A1) on the MCP23S08. This bit is not used on the MCP23008. The address pins are always enabled on the MCP23008.
- The Open-Drain (ODR) control bit enables/disables the INT pin for open-drain configuration.
- The Interrupt Polarity (INTPOL) control bit sets the polarity of the INT pin. This bit is functional only when the ODR bit is cleared, configuring the INT pin as active push-pull.

REGISTER 1-6: IOCON – I/O EXPANDER CONFIGURATION REGISTER (ADDR 0x05)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
—	—	SEQOP	DISSLW	HAEN	ODR	INTPOL	—
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'.

bit 5 **SEQOP:** Sequential Operation mode bit.
1 = Sequential operation disabled, address pointer does not increment.
0 = Sequential operation enabled, address pointer increments.

bit 4 **DISSLW:** Slew Rate control bit for SDA output.
1 = Slew rate disabled.
0 = Slew rate enabled.

bit 3 **HAEN:** Hardware Address Enable bit (MCP23S08 only).
Address pins are always enabled on MCP23008.
1 = Enables the MCP23S08 address pins.
0 = Disables the MCP23S08 address pins.

bit 2 **ODR:** This bit configures the INT pin as an open-drain output.
1 = Open-drain output (overrides the INTPOL bit).
0 = Active driver output (INTPOL bit sets the polarity).

bit 1 **INTPOL:** This bit sets the polarity of the INT output pin.
1 = Active-high.
0 = Active-low.

bit 0 **Unimplemented:** Read as '0'.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

1.6.7 PULL-UP RESISTOR CONFIGURATION (GPPU) REGISTER

The GPPU register controls the pull-up resistors for the port pins. If a bit is set and the corresponding pin is configured as an input, the corresponding port pin is internally pulled up with a 100 kΩ resistor.

REGISTER 1-7: GPPU – GPIO PULL-UP RESISTOR REGISTER (ADDR 0x06)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0
bit 7							bit 0

bit 7-0 **PU7:PU0:** These bits control the weak pull-up resistors on each pin (when configured as an input) <7:0>.

1 = Pull-up enabled.
0 = Pull-up disabled.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

1.6.8 INTERRUPT FLAG (INTF) REGISTER

The INTF register reflects the interrupt condition on the port pins of any pin that is enabled for interrupts via the GPINTEN register. A 'set' bit indicates that the associated pin caused the interrupt.

This register is 'read-only'. Writes to this register will be ignored.

Note: INTF will always reflect the pin(s) that have an interrupt condition. For example, one pin causes an interrupt to occur and is captured in INTCAP and INF. If, before clearing the interrupt, another pin changes which would normally cause an interrupt, it will be reflected in INTF, but not INTCAP.

REGISTER 1-8: INTF – INTERRUPT FLAG REGISTER (ADDR 0x07)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
bit 7							bit 0

bit 7-0 **INT7:INT0:** These bits reflect the interrupt condition on the port. Will reflect the change only if interrupts are enabled (GPINTEN) <7:0>.

1 = Pin caused interrupt.
0 = Interrupt not pending.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

1.6.9 INTERRUPT CAPTURE (INTCAP) REGISTER

The INTCAP register captures the GPIO port value at the time the interrupt occurred. The register is 'read-only' and is updated only when an interrupt occurs. The register will remain unchanged until the interrupt is cleared via a read of INTCAP or GPIO.

REGISTER 1-9: INTCAP – INTERRUPT CAPTURED VALUE FOR PORT REGISTER (ADDR 0x08)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ICP7	ICP6	ICP5	ICP4	ICP3	ICP2	ICP1	ICP0
bit 7							bit 0

bit 7-0 **ICP7:ICP0:** These bits reflect the logic level on the port pins at the time of interrupt due to pin change <7:0>.
1 = Logic-high.
0 = Logic-low.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

1.6.10 PORT (GPIO) REGISTER

The GPIO register reflects the value on the port. Reading from this register reads the port. Writing to this register modifies the Output Latch (OLAT) register.

REGISTER 1-10: GPIO – GENERAL PURPOSE I/O PORT REGISTER (ADDR 0x09)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0
bit 7							bit 0

bit 7-0 **GP7:GP0:** These bits reflect the logic level on the pins <7:0>.
1 = Logic-high.
0 = Logic-low.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

1.6.11 OUTPUT LATCH REGISTER (OLAT)

The OLAT register provides access to the output latches. A read from this register results in a read of the OLAT and not the port itself. A write to this register modifies the output latches that modify the pins configured as outputs.

REGISTER 1-11: OLAT – OUTPUT LATCH REGISTER 0 (ADDR 0x0A)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0
bit 7							bit 0

bit 7-0 **OL7:OL0:** These bits reflect the logic level on the output latch <7:0>.
1 = Logic-high.
0 = Logic-low.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

1.7 Interrupt Logic

The interrupt output pin will activate if an internal interrupt occurs. The interrupt block is configured by the following registers:

- GPINTEN – enables the individual inputs
- DEFVAL – holds the values that are compared against the associated input port values
- INTCON – controls if the input values are compared against DEFVAL or the previous values on the port
- IOCON (ODR and INPOL) – configures the INT pin as push-pull, open-drain and active-level

Only pins configured as inputs can cause interrupts. Pins configured as outputs have no affect on INT.

Interrupt activity on the port will cause the port value to be captured and copied into INTCAP. The interrupt will remain active until the INTCAP or GPIO register is read. Writing to these registers will not affect the interrupt.

The first interrupt event will cause the port contents to be copied into the INTCAP register. Subsequent interrupt conditions on the port will not cause an interrupt to occur as long as the interrupt is not cleared by a read of INTCAP or GPIO.

1.7.1 INTERRUPT CONDITIONS

There are two possible configurations to cause interrupts (configured via INTCON):

1. Pins configured for **interrupt-on-pin-change** will cause an interrupt to occur if a pin changes to the opposite state. The default state is reset after an interrupt occurs. For example, an interrupt occurs by an input changing from `1` to `0`. The new initial state for the pin is a logic `0`.
2. Pins configured for **interrupt-on-change from register value** will cause an interrupt to occur if the corresponding input pin differs from the register bit. The interrupt condition will remain as long as the condition exists, regardless if the INTAP or GPIO is read.

See Figure 1-6 and Figure 1-7 for more information on interrupt operations.

FIGURE 1-6: INTERRUPT-ON-PIN-CHANGE

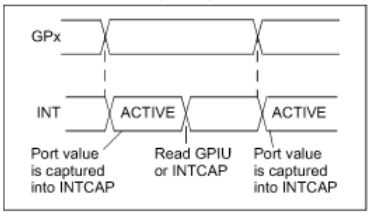
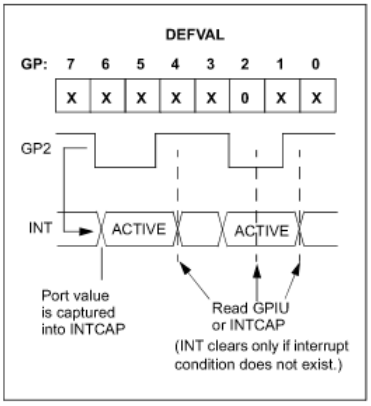


FIGURE 1-7: INTERRUPT-ON-CHANGE FROM REGISTER DEFAULT



NOTES:

2.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +5.5V
Voltage on all other pins with respect to V_{SS} (except V_{DD}) ..... -0.6V to (V_{DD} + 0.6V)
Total power dissipation (**Note**) ..... 700 mW
Maximum current out of V_{SS} pin ..... 150 mA
Maximum current into V_{DD} pin ..... 125 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Maximum output current sunk by any output pin ..... 25 mA
Maximum output current sourced by any output pin ..... 25 mA

Note: Power dissipation is calculated as follows:
$P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2.1 DC Characteristics

DC Characteristics		Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) **(Note 1)**					
Param No.	**Characteristic**	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	1.8	—	5.5	V	
D002	VDD Start Voltage to Ensure Power-on Reset	VPOR	—	VSS	—	V	
D003	VDD Rise Rate to Ensure Power-on Reset	SVDD	0.05	—	—	V/ms	Design guidance only. Not tested.
D004	Supply Current	IDD	—	—	1	mA	SCL/SCK = 1 MHz
D005	Standby current	IDDS	—	—	1	µA	
			—	—	2	µA	4.5V - 5.5V @ +125°C **(Note 1)**
	Input Low-Voltage						
D030	A0, A1 (TTL buffer)	VIL	VSS	—	0.15 VDD	V	
D031	$\overline{CS}$, GPIO, SCL/SCK, SDA, A2, $\overline{RESET}$ (Schmitt Trigger)		VSS	—	0.2 VDD	V	
	Input High-Voltage						
D040	A0, A1 (TTL buffer)	VIH	0.25 VDD + 0.8	—	VDD	V	
D041	$\overline{CS}$, GPIO, SCL/SCK, SDA, A2, $\overline{RESET}$ (Schmitt Trigger)		0.8 VDD	—	VDD	V	For entire VDD range.
	Input Leakage Current						
D060	I/O port pins	IIL	—	—	±1	µA	VSS ≤ VPIN ≤ VDD
	Output Leakage Current						
D065	I/O port pins	ILO	—	—	±1	µA	VSS ≤ VPIN ≤ VDD
D070	GPIO weak pull-up current	IPU	40	75	115	µA	VDD = 5V, GP Pins = VSS –40°C ≤ TA ≤ +85°C
	Output Low-Voltage						
D080	GPIO	VOL	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V
	INT		—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V
	SO, SDA		—	—	0.6	V	IOL = 3.0 mA, VDD = 1.8V
	SDA		—	—	0.8	V	IOL = 3.0 mA, VDD = 4.5V
	Output High-Voltage						
D090	GPIO, INT, SO	VOH	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V
			VDD – 0.7	—	—		IOH = -400 µA, VDD = 1.8V
	Capacitive Loading Specs on Output Pins						
D101	GPIO, SO, INT	CIO	—	—	50	pF	
D102	SDA	CB	—	—	400	pF	

Note 1: This parameter is characterized, not 100% tested.

FIGURE 2-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

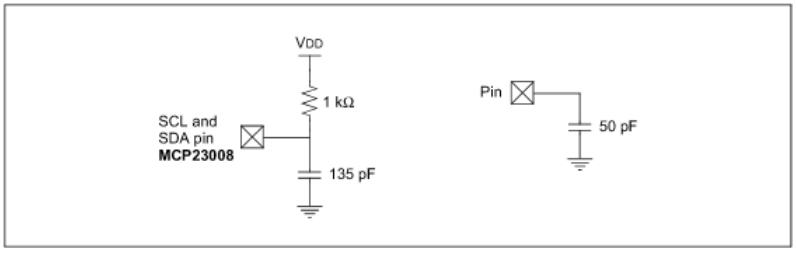


FIGURE 2-2: RESET AND DEVICE RESET TIMER TIMING

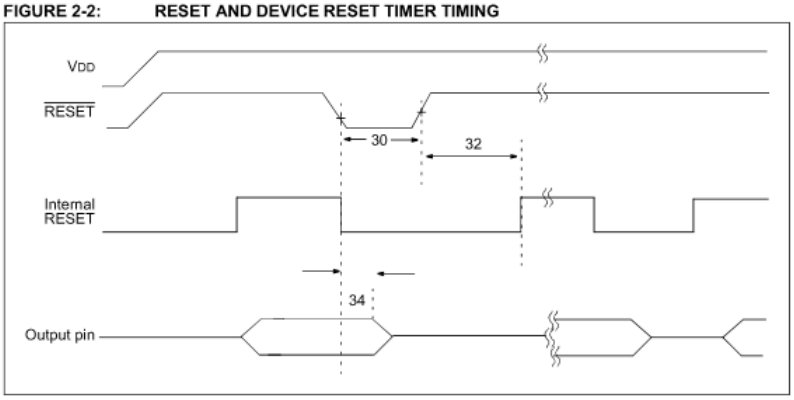


TABLE 2-1: DEVICE RESET SPECIFICATIONS

AC Characteristics		Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) **(Note 1)**					
Param No.	**Characteristic**	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
30	$\overline{\text{RESET}}$ Pulse Width (Low)	TRSTL	1	—	—	µs	
32	Device Active After Reset high	THLD	—		TBD	µs	VDD = 5.0V
34	Output High-Impedance From $\overline{\text{RESET}}$ Low	TIOZ	—	—	1	µs	

Note 1: This parameter is characterized, not 100% tested.

FIGURE 2-3: I²C™ BUS START/STOP BITS TIMING

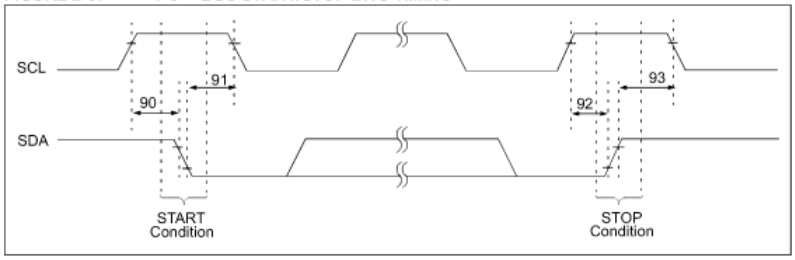


FIGURE 2-4: I²C™ BUS DATA TIMING

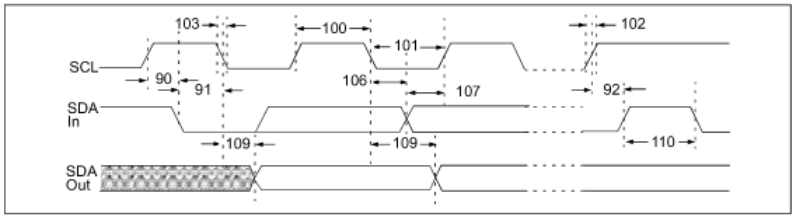


TABLE 2-2: I²C™ BUS DATA REQUIREMENTS (SLAVE MODE)

I²C™ AC Characteristics		Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) **(Note 1)** RPU (SCL, SDA) = 1 kΩ, CL (SCL, SDA) = 135 pF					
Param No.	**Characteristic**	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
100	Clock High Time:	THIGH					
	100 kHz mode		4.0	—	—	µs	1.8V – 5.5V (I-Temp)
	400 kHz mode		0.6	—	—	µs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0.12	—	—	µs	4.5V – 5.5V (E-Temp)
101	Clock Low Time:	TLOW					
	100 kHz mode		4.7	—	—	µs	1.8V – 5.5V (I-Temp)
	400 kHz mode		1.3	—	—	µs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0.32	—	—	µs	4.5V – 5.5V (E-Temp)
102	SDA and SCL Rise Time:	TR					
	100 kHz mode	**(Note 1)**	—	—	1000	ns	1.8V – 5.5V (I-Temp)
	400 kHz mode		20 + 0.1 CB(2)	—	300	ns	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		20	—	160	ns	4.5V – 5.5V (E-Temp)
103	SDA and SCL Fall Time:	TF					
	100 kHz mode	**(Note 1)**	—	—	300	ns	1.8V – 5.5V (I-Temp)
	400 kHz mode		20 + 0.1 CB(2)	—	300	ns	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		20	—	80	ns	4.5V – 5.5V (E-Temp)
90	START Condition Setup Time:	TSU:STA					
	100 kHz mode		4.7	—	—	µs	1.8V – 5.5V (I-Temp)
	400 kHz mode		0.6	—	—	µs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0.16	—	—	µs	4.5V – 5.5V (E-Temp)
91	START Condition Hold Time:	THD:STA					
	100 kHz mode		4.0	—	—	µs	1.8V – 5.5V (I-Temp)
	400 kHz mode		0.6	—	—	µs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0.16	—	—	µs	4.5V – 5.5V (E-Temp)
106	Data Input Hold Time:	THD:DAT					
	100 kHz mode		0	—	3.45	µs	1.8V – 5.5V (I-Temp)
	400 kHz mode		0	—	0.9	µs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0	—	0.15	µs	4.5V – 5.5V (E-Temp)
107	Data Input Setup Time:	TSU:DAT					
	100 kHz mode		250	—	—	ns	1.8V – 5.5V (I-Temp)
	400 kHz mode		100	—	—	ns	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0.01	—	—	µs	4.5V – 5.5V (E-Temp)
92	STOP Condition Setup Time:	TSU:STO					
	100 kHz mode		4.0	—	—	µs	1.8V – 5.5V (I-Temp)
	400 kHz mode		0.6	—	—	µs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0.16	—	—	µs	4.5V – 5.5V (E-Temp)

Note 1: This parameter is characterized, not 100% tested.

2: CB is specified to be from 10 to 400 pF.

TABLE 2-2: I²C™ BUS DATA REQUIREMENTS (SLAVE MODE) (CONTINUED)

I²C™ AC Characteristics			Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) **(Note 1)** RPU (SCL, SDA) = 1 kΩ, CL (SCL, SDA) = 135 pF				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
109	Output Valid From Clock:	TAA					
	100 kHz mode		—	—	3.45	µs	1.8V – 5.5V (I-Temp)
	400 kHz mode		—	—	0.9	µs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		—	—	0.18	µs	4.5V – 5.5V (E-Temp)
110	Bus Free Time:	TBUF					
	100 kHz mode		4.7	—	—	µs	1.8V – 5.5V (I-Temp)
	400 kHz mode		1.3	—	—	µs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		N/A	—	N/A	µs	4.5V – 5.5V (E-Temp)
	Bus Capacitive Loading:	CB					
	100 kHz and 400 kHz		—	—	400	pF	**(Note 1)**
	1.7 MHz		—	—	100	pF	**(Note 1)**
	Input Filter Spike Suppression: (SDA and SCL)	TSP					
	100 kHz and 400 kHz		—	—	50	ns	
	1.7 MHz		—	—	10	ns	Spike suppression off

Note 1: This parameter is characterized, not 100% tested.

2: CB is specified to be from 10 to 400 pF.

FIGURE 2-5: SPI™ INPUT TIMING

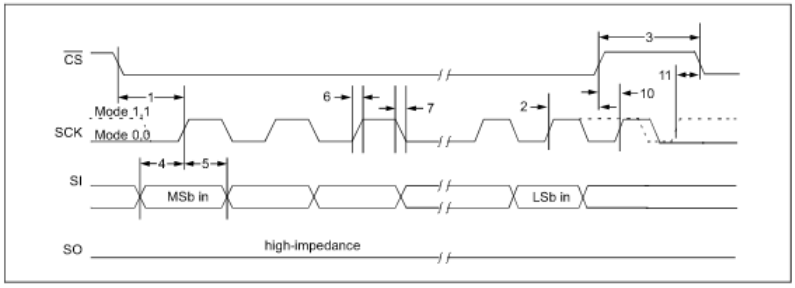


FIGURE 2-6: SPI™ OUTPUT TIMING

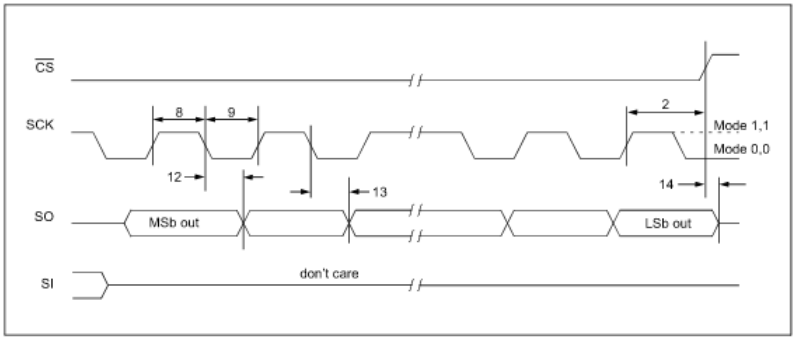


TABLE 2-3: SPI™ INTERFACE AC CHARACTERISTICS

SPI™ Interface AC Characteristics		Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) **(Note 1)**					
Param No.	**Characteristic**	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
	Clock Frequency	FCLK	—	—	5	MHz	1.8V – 5.5V (I-Temp)
			—	—	10	MHz	2.7V – 5.5V (I-Temp)
			—	—	10	MHz	4.5V – 5.5V (E-Temp)
1	$\overline{CS}$ Setup Time	TCSS	50	—	—	ns	
2	$\overline{CS}$ Hold Time	TCSH	100	—	—	ns	1.8V – 5.5V (I-Temp)
			50	—	—	ns	2.7V – 5.5V (I-Temp)
			50	—	—	ns	4.5V – 5.5V (E-Temp)
3	$\overline{CS}$ Disable Time	TCSD	100	—	—	ns	1.8V – 5.5V (I-Temp)
			50	—	—	ns	2.7V – 5.5V (I-Temp)
			50	—	—	ns	4.5V – 5.5V (E-Temp)
4	Data Setup Time	TSU	20	—	—	ns	1.8V – 5.5V (I-Temp)
			10	—	—	ns	2.7V – 5.5V (I-Temp)
			10	—	—	ns	4.5V – 5.5V (E-Temp)
5	Data Hold Time	THD	20	—	—	ns	1.8V – 5.5V (I-Temp)
			10	—	—	ns	2.7V – 5.5V (I-Temp)
			10	—	—	ns	4.5V – 5.5V (E-Temp)
6	CLK Rise Time	TR	—	—	2	µs	**Note 1**
7	CLK Fall Time	TF	—	—	2	µs	**Note 1**
8	Clock High Time	THI	90	—	—	ns	1.8V – 5.5V (I-Temp)
			45	—	—	ns	2.7V – 5.5V (I-Temp)
			45	—	—	ns	4.5V – 5.5V (E-Temp)

Note 1: This parameter is characterized, not 100% tested.

2: TV = 90 ns (max) when address pointer rolls over from address 0x0A to 0x00.

TABLE 2-3: SPI™ INTERFACE AC CHARACTERISTICS (CONTINUED)

SPI™ Interface AC Characteristics			Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) **(Note 1)**				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
9	Clock Low Time	TLO	90	—	—	ns	1.8V – 5.5V (I-Temp)
			45	—	—	ns	2.7V – 5.5V (I-Temp)
			45	—	—	ns	4.5V – 5.5V (E-Temp)
10	Clock Delay Time	TCLD	50	—	—	ns	
11	Clock Enable Time	TCLE	50	—	—	ns	
12	Output Valid from Clock Low	TV	—	—	90	ns	1.8V – 5.5V (I-Temp)
			—	—	45	ns	2.7V – 5.5V (I-Temp)
			—	—	45	ns	4.5V – 5.5V (E-Temp)
13	Output Hold Time	THO	0	—	—	ns	
14	Output Disable Time	TDIS	—	—	100	ns	

Note 1: This parameter is characterized, not 100% tested.

2: TV = 90 ns (max) when address pointer rolls over from address 0x0A to 0x00.

FIGURE 2-7: GPIO AND INT TIMING

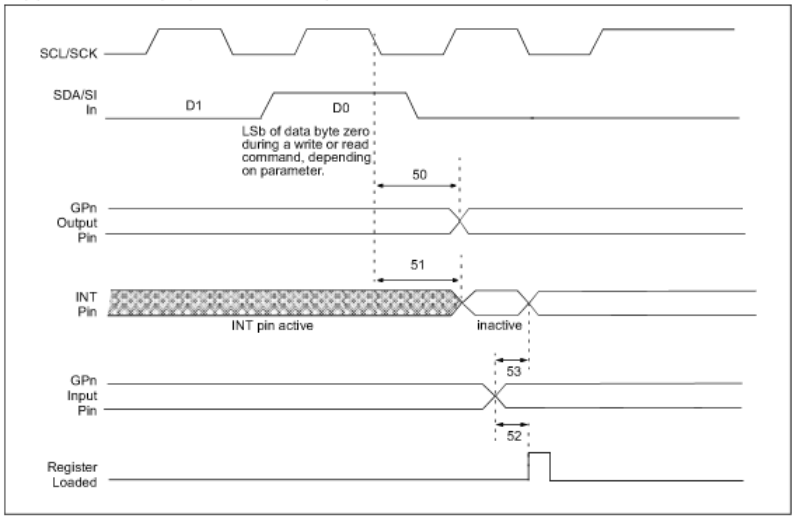


TABLE 2-4: GP AND INT PINS

AC Characteristics		Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) **(Note 1)**					
Param No.	**Characteristic**	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
50	Serial data to output valid	TGPOV	—	—	500	ns	
51	Interrupt pin disable time	TINTD	—	—	450	ns	
52	GP input change to register valid	TGPIV	—	—	450	ns	
53	IOC event to INT active	TGPINT	—	—	500	ns	
	Glitch Filter on GP Pins	TGLITCH	—	—	150	ns	

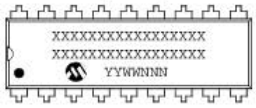
Note 1: This parameter is characterized, not 100% tested

NOTES:

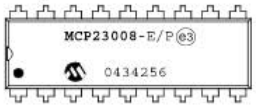
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

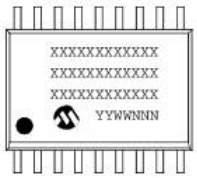
18-Lead PDIP (300 mil)



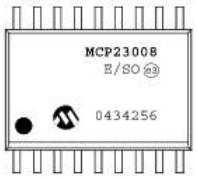
Example:



18-Lead SOIC (300 mil)



Example:



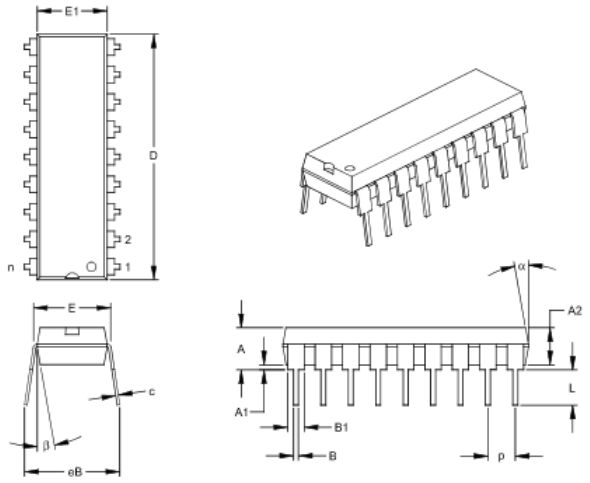
20-Lead SSOP

Example:

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

18-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

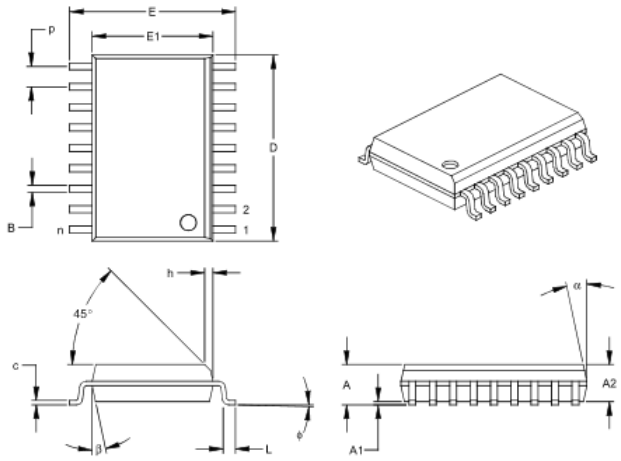


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.890	.898	.905	22.61	22.80	22.99
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-007

18-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

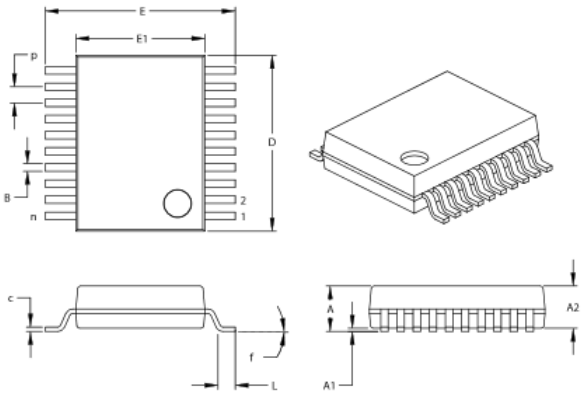


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.012	0.23	0.27	0.30
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-051

20-Lead Plastic Shrink Small Outline (SS) – 209 mil Body, 5.30 mm (SSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	P		.026			0.65	
Overall Height	A	-	-	.079	-	-	2.00
Molded Package Thickness	A2	.065	.069	.073	1.65	1.75	1.85
Standoff	A1	.002	-	-	0.05	-	-
Overall Width	E	.291	.307	.323	7.40	7.80	8.20
Molded Package Width	E1	.197	.209	.220	5.00	5.30	5.60
Overall Length	D	.272	.283	.289	.295	7.20	7.50
Foot Length	L	.022	.030	.037	0.55	0.75	0.95
Lead Thickness	c	.004	-	.010	0.09	-	0.25
Foot Angle	f	0°	4°	8°	0°	4°	8°
Lead Width	B	.009	-	.015	0.22	-	0.38

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-150

Drawing No. C04-072

Revised 11/03/03

APPENDIX A: REVISION HISTORY

Revision B (February 2005)

The following is the list of modifications:

1. **Section 1.6 "Configuration and Control Registers"**. Added Hardware Address Enable (HAEN) bit to Table 1-3.
2. **Section 1.6.6 "Configuration (IOCON) Register"**. Added Hardware Address Enable (HAEN) bit to Register 1-6.

Revision A (December 2004)

Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–	X	/XX
Device		Temperature Range	Package

Device	MCP23008:	8-Bit I/O Expander w/ I²C™ Interface
	MCP23008T:	8-Bit I/O Expander w/ I²C Interface (Tape and Reel)
	MCP23S08:	8-Bit I/O Expander w/ SPI™ Interface
	MCP23S08T:	8-Bit I/O Expander w/ SPI Interface (Tape and Reel)
Temperature Range	E =	-40°C to +125°C (Extended) *
	* While these devices are only offered in the "E" temperature range, the device will operate at different voltages and temperatures as identified in the **Section 2.0 "Electrical Characteristics"**.	
Package	P =	Plastic DIP (300 mil Body), 18-Lead
	SO =	Plastic SOIC (300 mil Body), 18-Lead
	SS =	SSOP, (209 mil Body, 5.30 mm), 20-Lead

Examples:

a) MCP23008-E/P: Extended Temp., 18LD PDIP package.
b) MCP23008-E/SO: Extended Temp., 18LD SOIC package.
c) MCP23008T-E/SO: Tape and Reel, Extended Temp., 18LD SOIC package.
d) MCP23008-E/SS: Extended Temp., 20LD SSOP package.
e) MCP23008T-E/SS: Tape and Reel, Extended Temp., 20LD SSOP package.

a) MCP23S08-E/P: Extended Temp., 18LD PDIP package.
b) MCP23S08-E/SO: Extended Temp., 18LD SOIC package.
c) MCP23S08T-E/SO: Tape and Reel, Extended Temp., 18LD SOIC package.
d) MCP23S08-E/SS: Extended Temp., 20LD SSOP package.
e) MCP23S08T-E/SS: Tape and Reel, Extended Temp., 20LD SSOP package.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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82-2-558-5934

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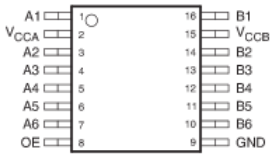
10/20/04

6-BIT BIDIRECTIONAL VOLTAGE-LEVEL TRANSLATOR WITH AUTO-DIRECTION SENSING AND ±15-kV ESD PROTECTION

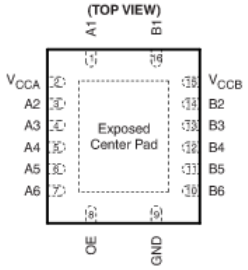
FEATURES

- 1.2 V to 3.6 V on A Port and 1.65 to 5.5 V on B Port ($V_{CCA} \leq V_{CCB}$)
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, All Outputs Are in the High-Impedance State
- OE Input Circuit Referenced to V_{CCA}
- Low Power Consumption, 4-μA Max I_{CC}
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - A Port
    - 2500-V Human-Body Model (A114-B)
    - 150-V Machine Model (A115-A)
    - 1500-V Charged-Device Model (C101)
  - B Port
    - ±15-kV Human-Body Model (A114-B)
    - 150-V Machine Model (A115-A)
    - 1500-V Charged-Device Model (C101)

PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



The exposed center pad, if used, must be connected as a secondary ground or left electrically open.

DESCRIPTION/ORDERING INFORMATION

This 6-bit noninverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes. V_{CCA} should not exceed V_{CCB}.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state.

The TXB0106 is designed so that the OE input circuit is supplied by V_{CCA}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

ORDERING INFORMATION

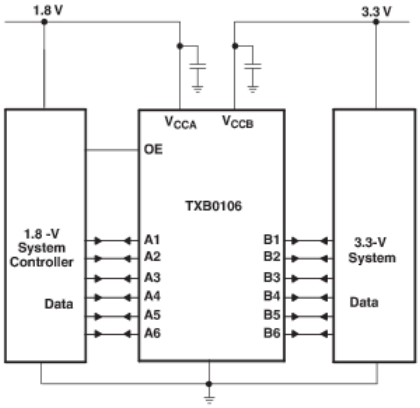
T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	TXB0106RGYR	YE06
	TSSOP – PW	Reel of 2000	TXB0106PWR	YE06

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN DESCRIPTION

NO.	NAME	FUNCTION
1	A1	Input/output 1. Referenced to V_{CCA}.
2	V_{CCA}	A-port supply voltage. 1.2 V ≤ V_{CCA} ≤ 3.6 V, V_{CCA} ≤ V_{CCB}.
3	A2	Input/output 2. Referenced to V_{CCA}.
4	A3	Input/output 3. Referenced to V_{CCA}.
5	A4	Input/output 4. Referenced to V_{CCA}.
6	A5	Input/output 5. Referenced to V_{CCA}.
7	A6	Input/output 6. Referenced to V_{CCA}.
8	OE	Output enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
9	GND	Ground
10	B6	Input/output 6. Referenced to V_{CCB}.
11	B5	Input/output 5. Referenced to V_{CCB}.
12	B4	Input/output 4. Referenced to V_{CCB}.
13	B3	Input/output 3. Referenced to V_{CCB}.
14	B2	Input/output 2. Referenced to V_{CCB}.
15	V_{CCB}	B-port supply voltage. 1.65 V ≤ V_{CCB} ≤ 5.5 V.
16	B1	Input/output 1. Referenced to V_{CCB}.

TYPICAL OPERATING CIRCUIT



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		–0.5	4.6	V
V_{CCB}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2)(3)	A inputs	–0.5	V_{CCA} + 0.5	V
		B inputs	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
$_{JA}$	Package thermal impedance	PW package(4)		83	°C/W
		RGY package(5)		37	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) The package thermal impedance is calculated in accordance with JESD 51-5.

RECOMMENDED OPERATING CONDITIONS(1)(2)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}					1.65	5.5	
V_{IH}	High-level input voltage	Data inputs	1.2 V to 3.6 V	1.65 V to 5.5 V	V_{CCI} × 0.65(3)	V_{CCI}	V
		OE			V_{CCA} × 0.65	5.5	
V_{IL}	Low-level input voltage	Data inputs	1.2 V to 5.5 V	1.65 V to 5.5 V	0	V_{CCI} × 0.35(3)	V
		OE	1.2 V to 3.6 V		0	V_{CCA} × 0.35	
$\Delta t/\Delta v$	Input transition rise or fall rate	A-port inputs	1.2 V to 3.6 V	1.65 V to 5.5 V		40	ns/V
		B-port inputs	1.2 V to 3.6 V	1.65 V to 3.6 V		40	
				4.5 V to 5.5 V		30	
T_A	Operating free-air temperature				–40	85	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, i.e., both at V_{CCI} or both at GND.
(2) V_{CCA} must be less than or equal to V_{CCB} and must not exceed 3.6 V.
(3) V_{CCI} is the supply voltage associated with the input port.

ELECTRICAL CHARACTERISTICS[1][2]

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V_{OHA}		I_{OH} = –20 µA	1.2 V			1.1				V
			1.4 V to 3.6 V					V_{CCA}– 0.4		
V_{OLA}		I_{OL} = 20 µA	1.2 V			0.9				V
			1.4 V to 3.6 V						0.4	
V_{OHB}		I_{OH} = –20 µA		1.65 V to 5.5 V				V_{CCB}– 0.4		V
V_{OLB}		I_{OL} = 20 µA		1.65 V to 5.5 V					0.4	V
I_I	OE		1.2 V to 3.6 V	1.65 V to 5.5 V			±1		±2	µA
I_{off}	A port		0 V	0 V to 5.5 V			±1		±2	µA
	B port		0 V to 3.6 V	0 V			±1		±2	
I_{OZ}	A or B port	OE = GND	1.2 V to 3.6 V	1.65 V to 5.5 V			±1		±2	µA
I_{CCA}		V_I = V_{CCI} or GND, I_O = 0	1.2 V	1.65 V to 5.5 V		0.06				µA
			1.4 V to 3.6 V						5	
			3.6 V	0 V					2	
			0 V	5.5 V					2	
I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	1.2 V	1.65 V to 5.5 V		3.4				µA
			1.4 V to 3.6 V						5	
			3.6 V	0 V					–2	
			0 V	5.5 V					2	
I_{CCA} + I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	1.2 V	1.65 V to 5.5 V		3.5				µA
			1.4 V to 3.6 V						10	
I_{CCZA}		V_I = V_{CCI} or GND, I_O = 0, OE = GND	1.2 V	1.65 V to 5.5 V		0.05				µA
			1.4 V to 3.6 V						5	
I_{CCZB}		V_I = V_{CCI} or GND, I_O = 0, OE = GND	1.2 V	1.65 V to 5.5 V		3.3				µA
			1.4 V to 3.6 V						5	
C_i	OE		1.2 V to 3.6 V	1.65 V to 5.5 V		5			5.5	pF
C_{io}	A port		1.2 V to 3.6 V	1.65 V to 5.5 V		5			6.5	pF
	B port					8			10	

(1) V_{CCI} is the supply voltage associated with the input port.
(2) V_{CCO} is the supply voltage associated with the output port.

TIMING REQUIREMENTS

T_A = 25°C, V_{CCA} = 1.2 V

			V_{CCB} = 1.8 V	V_{CCB} = 2.5 V	V_{CCB} = 3.3 V	V_{CCB} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
	Data rate		20	20	20	20	Mbps
t_w	Pulse duration	Data inputs	50	50	50	50	ns

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (unless otherwise noted)

			V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			50		50		50		50	Mbps
t_w	Pulse duration	Data inputs	20		20		20		20		ns

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

			V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			52		60		60		60	Mbps
t_w	Pulse duration	Data inputs	19		17		17		17		ns

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

			V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			70		100		100	Mbps
t_w	Pulse duration	Data inputs	14		10		10		ns

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

			V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
	Data rate			100		100	Mbps
t_w	Pulse duration	Data inputs	10		10		ns

SWITCHING CHARACTERISTICS

T_A = 25°C, V_{CCA} = 1.2 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V	V_{CCB} = 2.5 V	V_{CCB} = 3.3 V	V_{CCB} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
t_{pd}	A	B	9.5	7.9	7.6	8.5	ns
	B	A	9.2	8.8	8.4	8	
t_{en}	OE	A	1	1	1	1	µs
		B	1	1	1	1	
t_{dis}	OE	A	20	17	17	18	ns
		B	20	16	15	15	
t_{rA}, t_{fA}	A-port rise and fall times		4.1	4.4	4.1	3.9	ns
t_{rB}, t_{fB}	B-port rise and fall times		5	5	5.1	5.1	ns
$t_{sk(o)}$	Channel-to-channel skew		2.4	1.7	1.9	7	ns
Max data rate			20	20	20	20	Mbps

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.4	12.9	1.2	10.1	1.1	10	0.8	9.9	ns
	B	A	0.9	14.2	0.7	12	0.4	11.7	0.3	13.7	
t_{en}	OE	A		1		1		1		1	µs
		B		1		1		1		1	
t_{dis}	OE	A	6.6	33	6.4	25.3	6.1	23.1	5.9	24.6	ns
		B	6.6	35.6	5.8	25.6	5.5	22.1	5.6	20.6	
t_{rA}, t_{fA}	A-port rise and fall times		0.8	6.5	0.8	6.3	0.8	6.3	0.8	6.3	ns
t_{rB}, t_{fB}	B-port rise and fall times		1	7.3	0.7	4.9	0.7	4.6	0.6	4.6	ns
$t_{SK(O)}$	Channel-to-channel skew			2.6		1.9		1.6		1.3	ns
Max data rate			50		50		50		50		Mbps

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.6	11	1.4	7.7	1.3	6.8	1.2	6.5	ns
	B	A	1.5	12	1.2	8.4	0.8	7.6	0.5	7.1	
t_{en}	OE	A		1		1		1		1	µs
		B		1		1		1		1	
t_{dis}	OE	A	5.9	26.7	5.6	21.6	5.4	18.9	4.8	18.7	ns
		B	6.1	33.9	5.2	23.7	5	19.9	5	17.6	
t_{rA}, t_{fA}	A-port rise and fall times		0.7	5.1	0.7	5	1	5	0.7	5	ns
t_{rB}, t_{fB}	B-port rise and fall times		1	7.3	0.7	5	0.7	3.9	0.6	3.8	ns
$t_{SK(O)}$	Channel-to-channel skew			0.8		0.7		0.6		0.6	ns
Max data rate			52		60		60		60		Mbps

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.1	6.4	1	5.3	0.9	4.7	ns
	B	A	1	7	0.6	5.6	0.3	4.4	
t_{en}	OE	A		1		1		1	µs
		B		1		1		1	
t_{dis}	OE	A	5	16.9	4.9	15	4.5	13.8	ns
		B	4.8	21.8	4.5	17.9	4.4	15.2	
t_{rA}, t_{fA}	A-port rise and fall times		0.8	3.6	0.6	3.6	0.5	3.5	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.6	4.9	0.7	3.9	0.6	3.2	ns
$t_{sk(o)}$	Channel-to-channel skew			0.4		0.3		0.3	ns
Max data rate			70		100		100		Mbps

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A	B	0.9	4.9	0.8	4	ns
	B	A	0.5	5.4	0.2	4	
t_{en}	OE	A		1		1	µs
		B		1		1	
t_{dis}	OE	A	4.5	13.9	4.1	12.4	ns
		B	4.1	17.3	4	14.4	
t_{rA}, t_{fA}	A-port rise and fall times		0.5	3	0.5	3	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.7	3.9	0.6	3.2	ns
$t_{sk(o)}$	Channel-to-channel skew			0.4		0.3	ns
Max data rate			100		100		Mbps

OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA}							UNIT
			1.2 V	1.2 V	1.5 V	1.8 V	2.5 V	2.5 V	3.3 V	
			V_{CCB}							
			5 V	1.8 V	1.8 V	1.8 V	2.5 V	5 V	3.3 V to 5 V	
			TYP	TYP	TYP	TYP	TYP	TYP	TYP	
C_{pdA}	A-port input, B-port output	C_L = 0, f = 10 MHz, $t_r = t_f$ = 1 ns, OE = V_{CCA} (outputs enabled)	9	8	7	7	7	7	8	pF
	B-port input, A-port output		12	11	11	11	11	11	11	
C_{pdB}	A-port input, B-port output		35	26	27	27	27	27	28	
	B-port input, A-port output		26	19	18	18	18	20	21	
C_{pdA}	A-port input, B-port output	C_L = 0, f = 10 MHz, $t_r = t_f$ = 1 ns, OE = GND (outputs disabled)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.01	
C_{pdB}	A-port input, B-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.03	
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.03	

PRINCIPLES OF OPERATION

Applications

The TXB0106 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another.

Architecture

The TXB0106 architecture (see Figure 1) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a dc state, the output drivers of the TXB0106 can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction.

The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70 Ω at V_{CCO} = 1.2 V to 1.8 V, 50 Ω at V_{CCO} = 1.8 V to 3.3 V and 40 Ω at V_{CCO} = 3.3 V to 5 V.

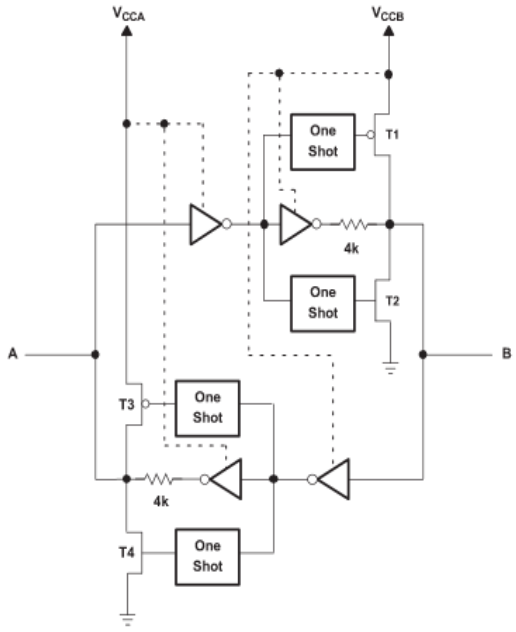
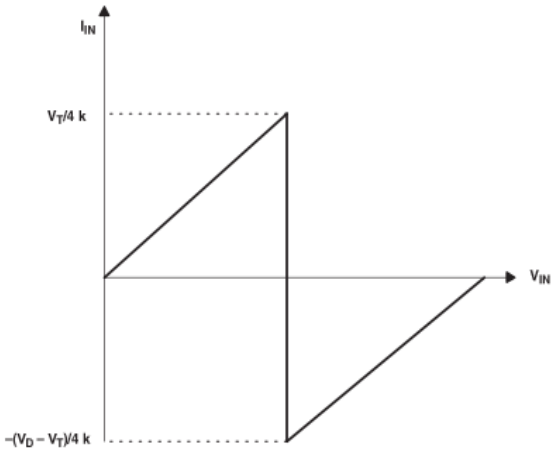


Figure 1. Architecture of TXB0106 I/O Cell

Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the TXB0106 are shown in Figure 2. For proper operation, the device driving the data I/Os of the TXB0106 must have drive strength of at least ±2 mA.



A. V_T is the input threshold voltage of the TXB0106 (typically $V_{CC}/2$).

B. V_D is the supply voltage of the external driver.

Figure 2. Typical I_{IN} vs V_{IN} Curve

Power Up

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. The TXB0106 has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B}$ = 0 V).

Enable and Disable

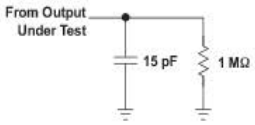
The TXB0106 has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

Pullup or Pulldown Resistors on I/O Lines

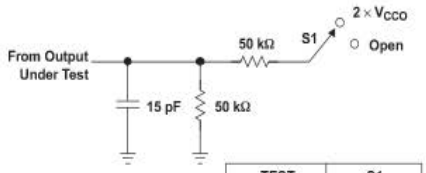
The TXB0106 is designed to drive capacitive loads of up to 70 pF. The output drivers of the TXB0106 have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 kΩ to ensure that they do not contend with the output drivers of the TXB0106.

For the same reason, the TXB0106 should not be used in applications such as I^2C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI TXS01xx series of level translators.

PARAMETER MEASUREMENT INFORMATION

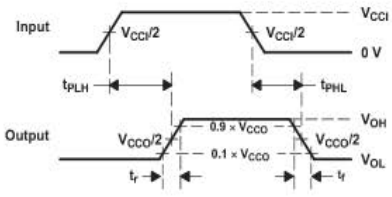


LOAD CIRCUIT FOR MAX DATA RATE, PULSE DURATION PROPAGATION DELAY OUTPUT RISE AND FALL TIME MEASUREMENT

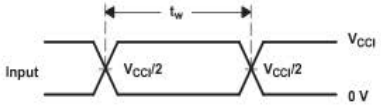


LOAD CIRCUIT FOR ENABLE/DISABLE TIME MEASUREMENT

TEST	S1
t_{PZL}/t_{PLZ}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS PULSE DURATION

A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. V_{CCI} is the V_{CC} associated with the input port.
F. V_{CCO} is the V_{CC} associated with the output port.
G. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuits and Voltage Waveforms

TEXAS INSTRUMENTS

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PACKAGE OPTION ADDENDUM

30-Jan-2012

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
TXB0106PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TXB0106PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TXB0106RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TXB0106RGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF TXB0106 :

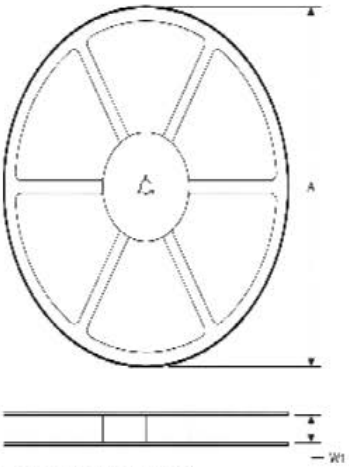
- Automotive: TXB0106-Q1

NOTE: Qualified Version Definitions:

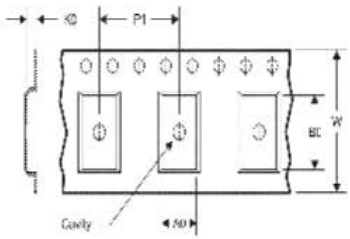
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



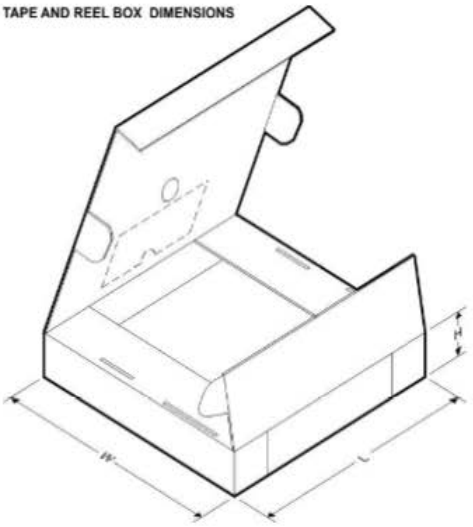
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0106PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TXB0106RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

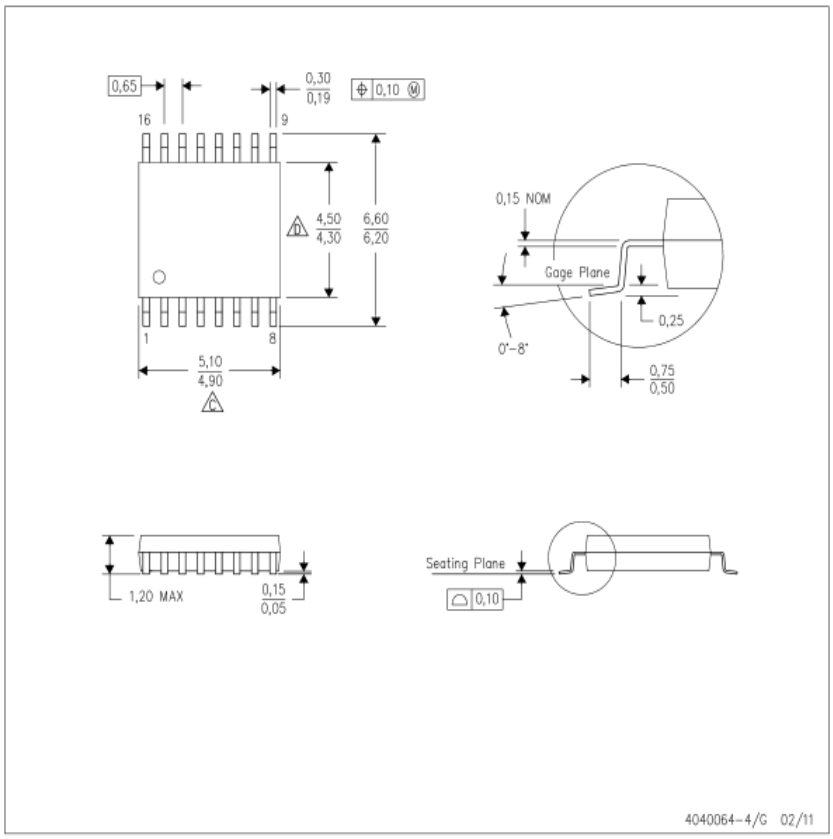
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0108PWR	TSSOP	PW	16	2000	346.0	346.0	29.0
TXB0106RGYR	VQFN	RGY	16	3000	346.0	346.0	29.0

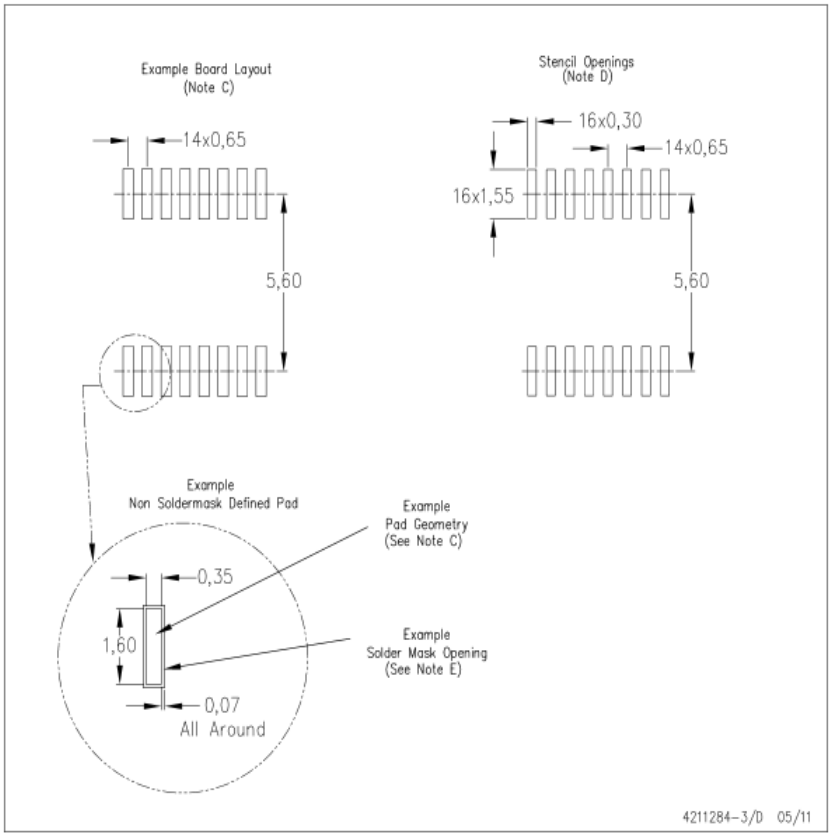
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

LAND PATTERN DATA

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

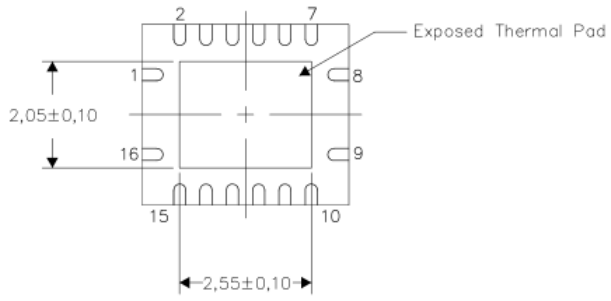
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



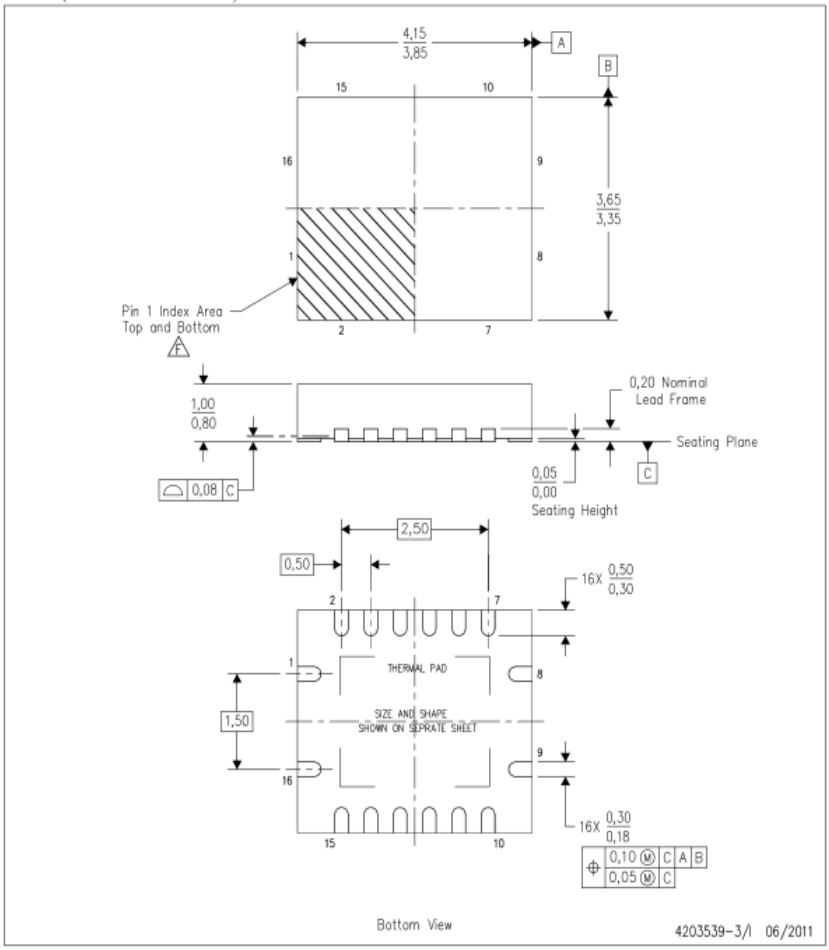
Bottom View

Exposed Thermal Pad Dimensions

4206353–3/0 11/11

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

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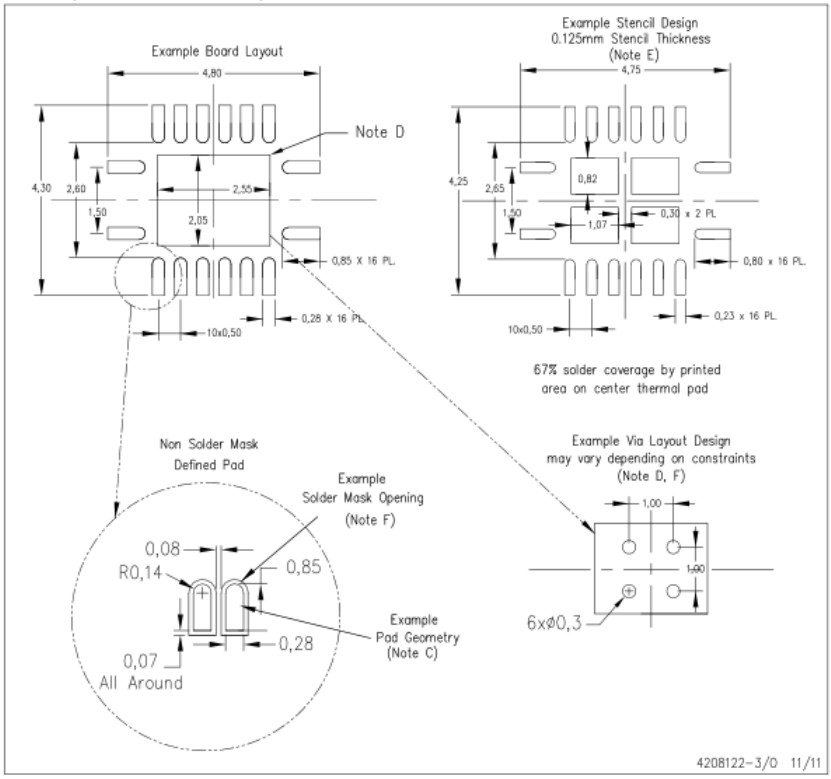
LAND PATTERN DATA

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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Appendix B – Operating Instructions

Neuronetrix	CONFIDENTIAL DESIGN DOCUMENT: All information contained herein is confidential and proprietary to Neuronetrix. Do not copy or distribute without prior written approval.		
TITLE: 7 ELECTRODE HEADSET TEST SYSTEM	RELEASE APPROVAL: Digitally signed by K.C. Fadem Reason: Document Release Date: 2013.05.15 10:08:58 -04'00'	CREATED BY: JIW	DATE CREATED: 1/24/2010
TYPE: PRODUCT SPEC		DOC NUMBER: PS-1487	REVISION: B

TABLE OF CONTENTS

1 PURPOSE

The purpose of this document is to specify the requirements and instructions necessary to test the COGNISION™ Headset with the 7-Electrode Headset Test System (PN-1572).

2 SCOPE

This document applies to the 7-Electrode Headset Test System and its software and associated tools when used to test the COGNISION™ Headset

3 RESPONSIBILITY AND AUTHORITY

Engineering is responsible for creating and maintaining this document

Manufacturing is responsible for following this document

4 TEST SPECIFICATIONS

4.1 Hardware Testing

Table 1

NO	TEST	SUB-SYS	DESCRIPTION	CONFIG	PROTOCOL	APPLICATION
1	**Current Draw**	ES, UY, HS, HCU	Measures current draw for nominal values, tests for shorts and abnormal functionality	All	n/a	CURRENT MONITORING
	Initialize Testset Open Master Control Panel Set Yoke Connection Control to HCU <-> Yoke (Turns off Testboard power to Yoke) Set frequency to 1 HZ Set DAC# update points to 90 Turn on current monitor Connect hardware to be tested according to the appropriate configuration diagram Turn on Testboard Check the current monitor to ensure that values do not exceed the specification If values exceed specification (12.1 below) turn off Testboard immediately to prevent damage to device					
6	**CAL Tones**	UY, ES, HS	Determines internal continuity and functioning CAL Tones	1, 2, 5, 6, 8	n/a	NOISE, CAL TONES & LOOPBACK
	Initialize Testset Open Noise, CAL Tones and Loopback Set COMM settings Set the proper configuration Click Start See section 12.3 below for results interpretation					

7	**Connectivity**	HS	to ensure all electrodes are properly connected to the Testset by injecting EEG_SIG and viewing YOKE_TX	1, 2, 5, 6	n/a	MASTER CONTROL PANEL
	Initialize Testset Open Master Control Panel Set COMM settings Set the MSBB UART COMMANDS to Sample every 8ms Click Send Command MSBB Wait for the signal to appear in the EEG display, check connections on test head if any signals are not displaying properly Close Master Control Panel					
8	**Baseline Noise**	HS	Measures internal "baseline" noise from Uberyoke and Electrode Strings by shorting amplifiers to ground	1, 2, 5, 6	n/a	NOISE, NOISE CAL TONES AND LOOPBACK
	Initialize Testset Open Noise, CAL Tones and Loopback Set COMM settings Set the proper configuration Click Start See 12.3 below for results interpretation					
10	**Baseline Offset**	HS	Shorts amplifier to ground, measures baseline offset	1, 2, 5, 6	n/a	NOISE
12	**Ambient Noise**	HS	Records the baseline noise of the test setup by monitoring channels without any signal being injected	1, 2, 5, 6	n/a	NOISE
13	**Crosstalk**	HS	Measures channel to channel crosstalk by injecting a large known signal into a channel and monitoring its effects on other channels outputs	1, 2, 5, 6	n/a	NOISE
	Initialize the Testset. Open the Crosstalk vi. Set the COMM settings. Set the proper configuration Click Start					
14	**CMRR**	HS	Inject a known signal into all electrodes then evaluate the EEG signal to establish the CMRR	1, 2, 5, 6	n/a	CMRR & FREQUENCY RESPONSE
	Initialize the Testset. Open the CMRR & Frequency Response vi. Set the COMM settings. Click the CMRR toggle. Set the proper configuration. Change the upper frequency bound to 60. Click Start See 12.5 below for results interpretation.					

15	**Settling Time**	HS	Time it takes for amplifiers to resettle after a voltage spike (artifact) has driven the amplifiers to a rail	1, 2, 5, 6	n/a	ARTIFACT
16	**DC Offset Tolerance**	HS	To evaluate the system's ability to tolerate an offset between the reference and electrodes	1, 2, 5, 6	n/a	MASTER CONTROL PANEL

Initialize the Testset

Open Master Control Panel.

Set the COMM settings.

Go to MSBB UART COMMANDS and Sample Every 8 ms.

Click Send Command MSBB.

Wait for the signal to stabilize.

Go to signal control and turn on Enable Offset.

A momentary change in the signal will occur when the offset is activated.

Starting with channel FZ activate the Bump/Offset FZ under bump and offset control.

The signal of a few channels will jump suddenly and then should resettle. Note: It may take up to a minute for the signals to resettle.

Go through each of the offsets, checking each channel for its tolerance to both negative and positive offsets.*

Go to MSBB UART COMMANDS and stop sampling.

Close the Master Control Panel

*Only use one offset at a time, the value of the offset will be divided among the number of offsets activated.

17	**Gain Linearity**	HS	To validate gain and gain linearity by injecting a spectrum of EEG voltages at a given frequency and record the output voltage. Enter gain offset into COGNISION™	1, 2, 5, 6	P_F009	GAIN LINEARITY, COGNISION™

Initialize Testset

Open Gain Linearity

Set COMM settings

Set the proper configuration

Click Start

See 12.6 below for results interpretation

18	**Frequency Response**	HS	To validate gain across a spectrum of frequencies by injecting a spectrum of EEG frequencies at a given voltage and recording the voltage attenuation	1, 2, 6	n/a	CMRR & FREQUENCY RESPONSE

Initialize the Testset.

Open CMRR & Frequency Response

Set COMM settings

Set the proper configuration

Click Start

See 12.4 below for results interpretation

22	**Keypad Test**	HCT	To ensure all buttons on the keypad work	4,7,8,9	n/a	HCU
23	**Button Test**	HCT	To validate user button functionality.	4,7,8,9	P_F008	HCU, COGNISION

24	**LED Test**	HCT	To ensure the LEDs visibly turn on and off.	4,7,8,9	n/a	HCU
26	**Power On**	HCT	To ensure that the unit will power ON.	5,6,8	n/a	HCU
27	**Power Off**	HCT	To ensure that the unit will power OFF.	5,6,8	n/a	HCU
28	**HCU USB Charge**	HCU	To ensure the HCU can charge via USB	7,8,12	IN-1706	SELF TEST
29	**Bluetooth Pairing**	HCU	To ensure that the unit will pair with an appropriately configured Bluetooth-enabled computer.	8,11,12	n/a	COGNISION™
	Log into COGNISION™ Open Test Admin. Select Manual Connect. Press discover When the HCU to be tested appears in the serial numbers box, select it and press connect. Once the blue connect light is illuminated on the HCU a connection has been established.					
53	**CAL Tone loopback**	UY, ES, HS	Determines Uberyoke internal continuity and basic functionality using CAL Tones	1, 2, 5, 6, 8	n/a	NOISE, CAL TONES & LOOPBACK
	Initialize the Testset. Open Noise, CAL Tones and Loopback. Set the COMM settings. Set the loopback toggle to ON. Click Start See 12.3 below for results.					
54	**HCU USB Connect**	HCU	To ensure the HCU can establish a USB connection with the computer	14	n/a	SIOW
55	**HCU LCD Test**	HCT	To ensure the HCU LCD screen displays properly	7,9	n/a	HCU

ES = Electrode String, HCU = Headset Control Unit, HCT = HCU Top, HS = Headset (Uberyoke + Electrode Strings), UY = Uberyoke, FW = Firmware

4.2 Firmware Testing

Table 2

NO	TEST	SUB	DESCRIPTION	CONFIG	PROTOCOL	Program
2	**Firmware Load - UY**	UY, HS	To initially load firmware or update firmware. VI loads firmware via programmer.	2	n/a	FIRMWARE LOAD PANEL
	1. Initialize the Testset 2. Open the Firmware Load Panel 3. Set the COMM settings 4. Set the test type to load target 5. Set program device to Uberycke 6. If this is the first time loading firmware, input the serial number 7. Click Start 8. Results will display with a failure or success message					
3	**Firmware Check - UY**	UY, HS	Update firmware, checks to make sure firmware can be upgraded, and ensures firmware is up to date	2	n/a	ICD & Master Panel & SIOW
4	**Firmware Check - HCU**	HCU	Update firmware, checks to make sure firmware can be upgraded, and ensures firmware is up to date	4, 5, 6, 7	n/a	COGNISION, SIOW
5	**Commands - UY**	UY	Execute each command available in succession, wait for OK from Uberycke	2, 5, 6	n/a	FIRMWARE
22	**Keypad Test**	HCT	To ensure all buttons on the keypad work	n/a	IN-1706	SELF TEST
23	**Button Test**	HCT	To validate user button functionality.	n/a	IN-1706, P_F008	SELF TEST
24	**LED Test**	HCT	To ensure the LEDs visibly turn on and off.	n/a	IN-1706	SELF TEST
25	**LCD Test**	HCT	To ensure all pixels on the LED turn on and off and without ghosts	n/a	IN-1706	SELF TEST
26	**Power On**	HCT	To ensure that the unit will power ON.	n/a	n/a	n/a
27	**Power Off**	HCT	To ensure that the unit will power OFF.	n/a	n/a	n/a
30	**Firmware Update**	FW	To validate proper function of the FUS.	12	n/a	FIRMWARE LOAD PANEL
31	**HCU Firmware Test**	FW	Execute each command available in succession, wait for OK from HCU	6,12	n/a	FIRMWARE
32	**HCU SELF TEST**	HCU, FW, HCT	Initiates a test mode that checks all the logic associated with the HCU Top: LEDs flash, keypad button check, button check, and LCD check in addition to battery charging and Uberycke current draw.	n/a	n/a	IN-1706
33	**No SSS**	FW	To ensure that the unit will generate the appropriate error if a test is to be initiated without an SSS loaded.	n/a	n/a	HCU
34	**SSS Download**	FW	To ensure that a validated SSS can be downloaded into the HCU.	n/a	P_F001	HCU
35	**Complete Protocol – Error Checking Disabled**	FW	To exercise a complete ERP configuration and upload data. Also tests sound from both earphones. Error checking disabled.	n/a	P_F001	HCU
36	**User Cancel Detection**	FW	To ensure that the unit exits the current ERP configuration when user presses 'Cancel' for 3 seconds.	n/a	P_F001	HCU
37	**Complete Two Configurations – Error Checking Disabled**	FW	To ensure that the unit loads second configuration successfully after the end of the first configuration.	n/a	P_F010	HCU
38	**MAX RESTING DURATION**	FW	To ensure a test failure when MAX RESTING DURATION is exceeded.	n/a	P_F002	HCU
39	**RESTING THRESHOLD DETECTION**	FW	To ensure that RESTING THRESHOLD DETECTION is functional when value is exceeded.	n/a	P_F002	HCU
40	**ARTIFACT THRESHOLD Detection**	FW	To ensure that errors are generated when ARTIFACT THRESHOLD is exceeded.	n/a	P_F003	HCU
1	**IMPEDANCE THRESHOLD Detection**	FW	To ensure that impedance ranges are functional and errors are generated when IMPEDANCE THRESHOLD is exceeded.	n/a	P_F004	HCU
42	**MAX ERRORS Failure**	FW	To ensure that a test failure will occur when MAX ERRORS is exceeded.	n/a	P_F005	HCU

43	**MAX TOTAL TEST DURATION Failure**	FW	To ensure that a test failure will occur when MAX TOTAL TEST DURATION is exceeded.	n/a	P_F006	HCU
44	**RESET ON ERROR Looping**	FW	To validate the looping function when RESET ON ERROR is enabled.	n/a	P_F007	HCU
50	**Epoch Set Replay on ARTIFACT THRESHOLD or IMPEDANCE THRESHOLD error.**	FW	To validate that when an ARTIFACT THRESHOLD or IMPEDANCE THRESHOLD error occurs, the entire Epoch Set is replayed.	n/a	P_F011	HCU
56	**Firmware Load – HCU**	HCU	Initial firmware load, checks to make sure firmware can be loaded, and ensure firmware is up to date.	4,5,6,7	n/a	FIRMWARE LOAD PANEL

1. Initialize the Testset.
2. Open the Firmware Load Panel.
3. Set the COMM settings.
4. Set the test type to load target.
5. Set Program Device to HCU
6. Click Start

Results will display with a failure or success message

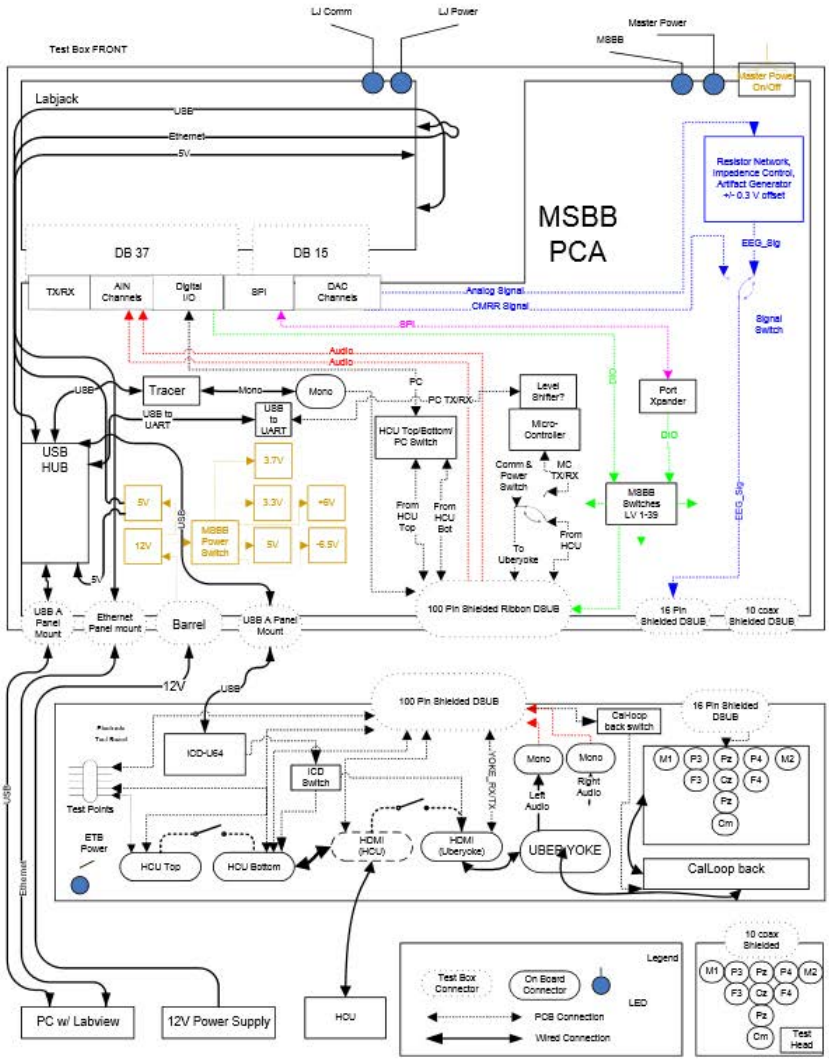
4.3 Audio Testing

Table 3

NO	TEST	SUB	DESCRIPTION	CONFIG	PROTOCOL	*APPLICATION*
19	**Audio Frequency**	AUD	To validate the precision and accuracy of the audio frequency, between 250 and 8000Hz	n/a	n/a	AUDIOSYS
20	**Volume Level**	AUD	To validate the precision and accuracy of the audio volume. Enter volume offset on COGNISION™	n/a	n/a	AUDIOSYS
21	**Volume Level Control**	AUD	To validate that the device will play a low volume without any initial or trailing pops	n/a	n/a	AUDIOSYS
46	**AUDIOMETRIC THRESHOLD DETECTION**	FW	To validate that the audiometry protocol can properly detect the hearing threshold of the patient, and properly compensate for it.	n/a	n/a	SOUND TEST
47	**Audio frequency**	FW	To validate the precision and accuracy of the audio frequency	n/a	P_F013	HCU AUDIO
48	**THRESHOLD COMPENSATION BAND**	FW	To validate that AUDIOMETRIC THRESHOLD DETECTION is using the THRESHOLD COMPENSATION BAND	n/a	n/a	SOUND
49	**DEFICIT VOLUME COMPENSATION**	FW	To validate that the earphone audio is adjusted based on the DEFICIT VOLUME COMPENSATION parameter	n/a	n/a	SOUND
51	**Audio Calibration**	FW	Calibrate the Test System's audio input by setting an offset voltage	n/a	n/a	AUDIOSYS
52	**Volume Level**	FW	To validate that the HCU can properly set Uberyoke volume	n/a	n/a	SOUND

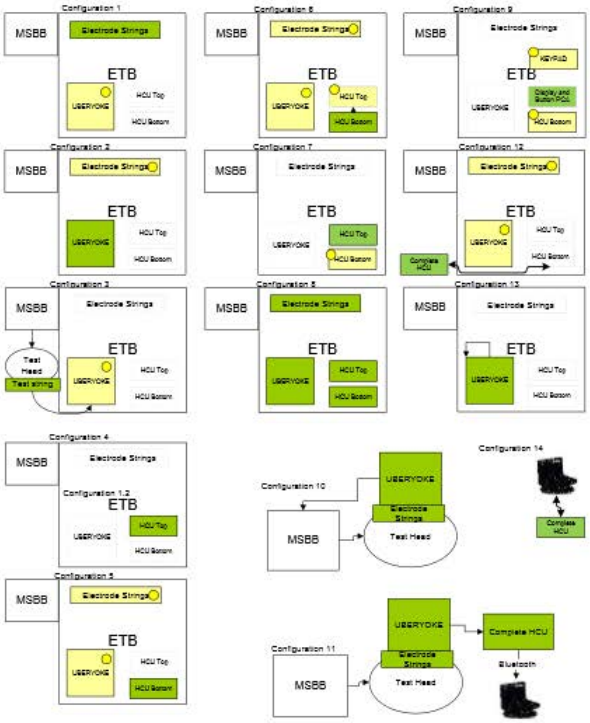
EB = Electrode String, HCU = Headset Control Unit, HCT = HCU Top, HS = Headset (Uberyoke + Electrode Strings), UY = Uberyoke, FW = Firmware

5 BLOCK DIAGRAM



6 TESTSET CONFIGURATION

6.1 Configurations DWG



Part Number	Descriptions
PN-1361	Keypad
PN-1513	HCU Top
PN-1515	HCU
PN-1509	Uberyoke PCA
PN-1212	Display and Button PCA
PN-1492	HCU Main Board
PN-1524	Headset
PN-1517,1519, 1521	Electrode Strings

7 SPECIFICATIONS

7.1 EEG Outputs

7.1.1 EEG Channels

- EEG Channel #: FZ (1), CZ (2), PZ(3), F3(4), P3(5), F4 (6), P4 (7)
- REF: M1, M2
- COM: C

7.1.2 EEG Output Signals:

- Wave profile: Sine, Flat, Ramp, Triangle
- Amplitude (µV): 0-380.0
- Frequency (Hz): 0-100.0

7.2 MISC. Outputs

7.2.1 CMRR Output Signal:

- Wave profile: Sine, Flat, Ramp, Triangle
- Amplitude (V): 0-±3 (± x)
- Frequency (Hz): 0-100 (± x)

7.2.2 Artifacts

- Amplitude: 200µV, 200mV
- Polarity: POS, NEG

7.2.3 Offset Voltage

- Amplitude: 0.3V
- Polarity: POS, NEG

7.3 Indicators

Indicators listed from left to right

- Labjack power
- Labjack COMM
- MSBB power
- Master power
- Electrode Test Board power

7.4 Software Controlled Switches & Settings

7.4.1 Switch: control & power from HCU to PC

7.4.2 Switch: HCU Top to HCU Bottom, HCU Top to PC or HCU Bottom to PC

7.4.3 Switches to select EEG signal: connect F3, P3, FZ, CZ, PZ, F4, P4

7.4.4 Switches for impedance selection: 0.5K, 20K, 56K, 76K

7.4.5 Firmware for setting ref impedance: 0.5K, 20k, 56k, 76k

7.4.6 Firmware for artifact control

- Artifact magnitude: 0-200µV, 0-200mV
- Artifact polarity: +Pos, -Neg
- Individual channel control for artifact injection: (On/off)

7.4.7 Firmware for offset control

- Offset (On/off)
- Offset polarity: +Pos, -Neg
- Individual channel control for offset injection: (On/off)

7.4.8 CMRR signal enable

Table 4 Software Communication

Software Suite Name		Description	Communication Method
CCS		Firmware programmer	ICD-U64
COGNISION™		ERP application	Bluetooth
SIOW		Terminal application	USB
FT_PROG		FTDI USB chip programming tool	USB
LabVIEW		Custom software applications	Bluetooth, USB, Ethernet
	Driver VI	Manually control any and all settings	
	Utility VI	Purpose built VI performs a specific task	
	Test VI	Executes an individual test from start to finish	
	Master VI	Executes multiple tests (a protocol) without user intervention	
	Launcher	The Top Level VI for launching all other VIs	

8 TESTSET VALIDATION

- Before starting the validation procedure, remove the HCU, Uberyoke and Electrode Strings from the Testset.
- Run Initialize VI 10.6.4
- Open the Master Control Panel and set the COMM settings
- Click run
- Testset should be configured so all test voltages are in an unloaded state.

Table 5

Testing at Test Points			
Testpoint Name	Expected Value	Tolerance or Range	Example values
Voltage Test Points			
POS6VOUT – YK	+6.3	±0.5	6.16V
NEG6VOUT – YK	-6.1	±0.5	-6.53V
HCU5VCRG	+5V	±0.5	4.98V
3.7VHCBT	+3.7V	±0.5	3.81V
+12VEX	+12V	±0.5	12.23V
-12VEX	-12V	±0.5	-12.48V
EXTEEG	The EXTEEG is checked using the oscilloscope and the voltmeter.		
	Amplitude@20Hz Volts@±LabVIEW setting 1.25V@±25mV 2.50V@±50mV 5.00V@±100mV 10.0V@±200mV 20.0V@±400mV (signal clipped)	 Volts@±LabVIEW setting 1.25V±0.01 2.50V±0.1 5.0V±0.2 10.1V±0.2 20.0V±0.2 (signal clipped)	 1.26V 2.56V 5.12V 10.1V 20.0V (signal clipped)
	Amplitude: Set the frequency to 20Hz Set the amplitudes to ± 25mV Set the wave shape to sine Turn on all channels Using the oscilloscope attach the ground to the GND test point Using the oscilloscope place the probe at the EXTEEG test point Measure the amplitude using the cursors Increment the amplitude through each of the designated amplitudes.		
	Frequency 10 Hz 20 Hz 40 Hz 80 Hz	 10.000±0.00 20.000±0.001 40.00±0.01 80.00±0.01	n/a
	Frequency: Set the amplitude to ± 100 µV Set the frequency to 10Hz Using the oscilloscope attach the ground to the GND test point Using the oscilloscope place the probe at the EXTEEG test point Read the frequency from the oscilloscope Increment the frequency through each of the designated frequencies		

	DC Offset 0.0V	 0.005V	 0.002V
	Set the amplitude to ± 100mV Set the frequency to 20Hz Measure the offset by placing the voltmeter probes on the GND and EXTEEG test points.		
EXTCOMSIG	The EXTCOMSIG is checked using the oscilloscope and the voltmeter.		
	Amplitude Volts@±LabVIEW setting 375mV@±25mV 750mV@±50mV 1.5V@±100mV 3.0V@±200mV 6.0V@±400mV (clipped)	 375mV±10mV 750mV±10mV 1.50V±0.1V 3.00V±0.1V 5.00V±0.1V	 382mV 752mV 1.5V 3.06V 5.96V (clipped)
	Amplitude: Set the frequency to 20Hz Set the amplitudes to ± 25mV Set the wave shape to sine Turn on all channels Using the oscilloscope attach the ground to the GND test point Using the oscilloscope place the probe at the EXTCOMSIG test point Measure the amplitude using the cursors Increment the amplitude through each of the designated amplitudes		
	Frequency 10 Hz 20 Hz 40 Hz 80 Hz	 10.000±0.001 20.000±0.001 40.00±0.01 80.00±0.01	n/a
	Frequency: Set the amplitude to ± 100 Set the frequency to 10Hz Using the oscilloscope attach the ground to the GND test point Using the oscilloscope place the probe at the EXTCOMSIG test point Read the frequency from the oscilloscope Increment the frequency through each of the designated frequencies		
	DC Offset 0.0V	 0.5	 0.53V
	Set the amplitude to ± 100mV Set the frequency to 20Hz Measure the offset by placing the voltmeter probes on the GND and EXTCOMSIG test points.		
Input			
	UART		
	Audio		
	Testing at Electrodes		
Impedances @Electrodes			
	0.5k	Signal Ch 85.5 ±0.5 Ref Ch 36.5 ±0.5 Com Ch ""	
	20k	Signal Ch 20.0 ±0.5 Com Ch 20.0 ±0.5	
	56k	Signal Ch 56.0 ±0.5 Com Ch 56.0 ±0.5	

	76k	Signal Ch 75.9 ±0.2 Com Ch 76.0 ±0.2	
	Impedance: Set all channels' impedance to 0.05k Place the negative probe on the com electrode pin Check each of the other electrode pins (including the ref pins) with the positive probe Set all channels' impedance to 20k Set the com channel to 0.05V Place the negative probe on the com electrode pin Check each of the other electrode pins (including the ref pins) with the positive probe. Repeat this procedure for 56k and 76k. To check the com's impedance set FZ's impedance to 0.05k then vary the impedance of the com using the positive probe to check the com and the negative probe placed on FZ.		
DC Offset			
	0.3 V	±.05	.2929 V
	-0.3 V	±.05	-.2928 V
	Turn off all Signals Enable the Offset from Signal control Using the voltmeter, place the negative probe on reference M1 In turn, one by one, enable and disable each of the Bump/Offset controls, using the positive probe to test each of the electrode pins on the test board that corresponds with that bump/offset control. Repeat the procedure with the Offset NEG Polarity control engaged.		
Artifact Generation			
	+200µV	±5%	
	-200µV	±5%	
	+200mV	±5%	
	-200mV	±5%	
EEG			
Amplitude	750 µV pk-pk 100 µV pk-pk	±5%	
Offset	<30 µV pk-pk		
CMRR			
Amplitude	5.5 V		
Test Head Continuity			
	<2.0 Ω		1.5 Ω
	Disable all channels Using the ohmmeter (continuity tester) test the continuity between the test head and the testboard electrode pins. Place one probe on the com electrode pin of the test board, then place the other probe on the copper ring of the com contact on the test head. Repeat this process for each corresponding electrode pin test head contact pair.		
Check List			
	Switch Path	Contact Points	Ω or V
Signal Switching	Establish that all switches are functional by assessing continuity or voltage differential		
	Enable HCU battery charge	Check for voltage when battery charge is enabled	

		5VCHG TP to GND TP*	4.98 V
	Enable MSB to HCU power	Check for voltage when MSB to HCU power is enabled	
		3.7V VHCBT to GND TP	3.98 V
	Enable HCU top to bottom power	Check for continuity between the connectors when switch is enabled	
		J19 pins 53-56 to j20 pins 53-56	<1 Ω
	Loopback enable	Check for continuity between connectors when switch is enabled	
		YK-CAL-3-POS @ J7 pin 2 to: YK-SIG-CH-P3 @ J7 pin 3 YK-SIG-CH-F3 @ J7 pin 4 YK-SIG-CH-PZ @ J8 pin 3 YK-SIG-CH-CZ @ J8 pin 4 YK-SIG-CH-FZ @ J8 pin 5 YK-SIG-CH-P4 @ J9 pin 3 YK-SIG-CH-F4 @ J9 pin 4	100 KΩ ±0.5 KΩ
		YK-CAL-4-NEG @ J9 pin 2 to: YK-SIG-REF-L @ m2 pin 3 YK-SIG-REF-R @ M1 pin 3	100 KΩ ±0.5 KΩ
	LCD enable	Check for 3.3V voltage when switch is enabled	
		J19 pin 2 & 4 to J20 pin 2 & 4	<3 Ω closed <40M Ω open
	Yoke connection switches	Check if the HCU to Yoke connection is interrupted	
		J13 2,3,12,13 to J22 2,3,12,13	<0.5 Ω
	HCU connection switches	Check if HCU top to bottom is interrupted	
		J19 pins 1, 3, 5, 7, 9, 11, 13, 16, 18, 20, 22 to J20 pins 1, 3, 5, 7, 9, 11, 13, 16, 18, 20, 22	<3 Ω
	Programmer connection switches	RLY1 pin 2 to RLY1 pin 3 RLY1 pin 7 to RLY1 pin 6 RLY2 pin 2 to RLY2 pin 3 RLY2 pin 7 to RLY2 pin 6	<1 Ω
*TP = Test Point			

9 Maintenance

9.1 Some parts of the Testset are prone to wear and should be inspected and replaced as necessary.

9.1.1 Testboard

- Electrode and Uberyoke Testboard Headers : Inspect the connectors, replace if they are over worn or broken
- Rubber hold down stoppers : Inspect the stoppers, replace if they are overly worn.
- Inspect connectors and plastic parts : replace if they are broken.

9.1.2 TestHead

- Electrode contacts : Inspect the contacts, replace if they are worn or broken.

10 LABVIEW Vis

10.1 LabVIEW Hierarchy

10.1.1 Interface Hierarchy - Master Test - > Test Panel > Master Control Panel -> SubVI's > Driver access VI's

10.1.2 Control Hierarchy – Panel -> Cluster (Common) -> Control

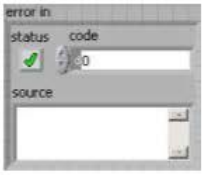
10.2 COMM Settings Cluster (Common)

10.2.1 Any test, or function panel that communicates with the MSBB will have a COMM Settings cluster associated with it. It may be off screen above the controls. This panel contains the necessary information to establish a connection with the MSBB. The panel has two occurrences, an input and an output. The output cluster is grayed out, and modification will have no effects on the program. The output cluster displays the information that was passed to other function panels. The input cluster will affect the program function, it's information propagates through the program.

Table 6

I/O	Value	Example	Description
Input	IP address	192.168.1.200	This is the IP address for the Labjack located in the MSBB, this is settable in the Labjack control panel.
Input	Connection Type	LJ_ctEthernet / LJ_ctUSB	This is the method used to connect to the Labjack located in the MSBB, the options are USB and Ethernet, and allows for use across the network, however USB is especially useful when troubleshooting connection problems.
Input	Handle	156158768	Only an input during development, used by the developer if the VI doesn't generate its own, this is used to pass the Labjack reference from one function to another.
Input	File path	C:\Headset Test System\logs	If the user is going to log files this path needs to be populated with the root directory for the logs.
Input	Visa Resource	COM50	Drop down menu, selects port address for the UART

10.3 Error Reporting Cluster (Common)



10.3.1 Any VI that interacts with hardware will have an error input and output. The error code is generated at the bottom level VI and propagated from there. Most errors will terminate the program. Errors #'s between 6000-8000 are Labjack associated, for a list of these errors see the Labjack ue9 users manual under error codes. The error display is a cluster of 3 components. A status marker, green arrow or red x, a code window that will display the code, and a source window which will contain the first place the error was detected.

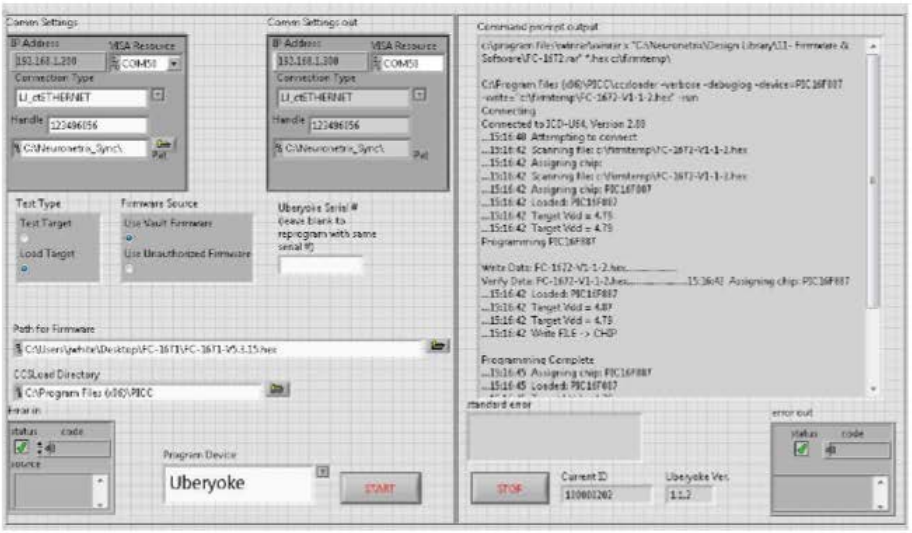
Table 7

Error Code	Description	Cause(s)	Solution
7/6007	Stream error,	Too high of a frequency selected	Lower the frequency or lower the number of update points

8/6008	Buffer overrun while streaming	Current monitor run at too high of a frequency	Lower the frequency, lower the number of update points
1000/7008	1008 is an unknown error, and can generally be ignored;	Most frequently caused by changing settings too fast	Restart task, change the settings at a slower rate

10.4 Firmware Load

10.4.1 Purpose –To provide a robust method of programming firmware for the various devices associated with the COGNISION™ system. Provides a fast, automated method that reduces the chance of improperly loading firmware. This panel is versatile in that it can test a target chip, or load firmware onto it. The firmware can be obtained from an authorized source, or can be if the user chooses, loaded from an optional location.



10.4.2 Inputs/controls

Table 8

	Control	Description	State(s)
	COMM	MSBB communication	(See 10.2 above)
	Test Type	Selects whether to test the target or load firmware into the target	Test Target Load Target
	Firmware Source	Select whether the file used is the version in the vault or from a user specified location	Use Vault Firmware Use Unauthorized Firmware

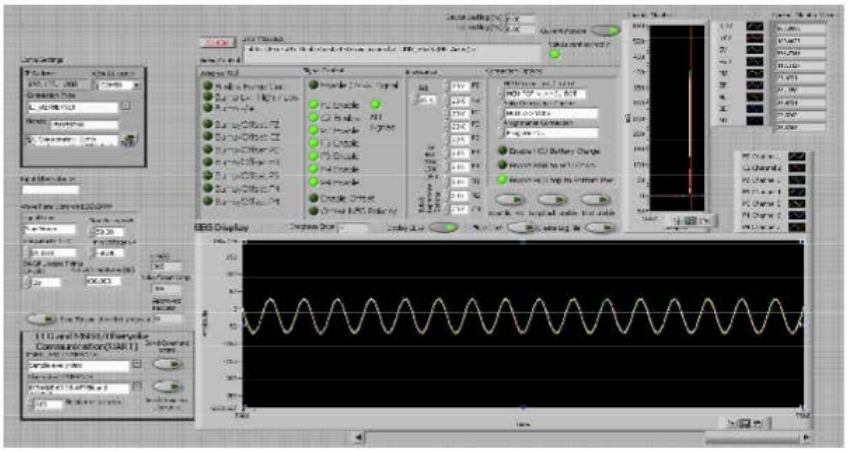
	Uberyoke Serial #	If this is a first load for the Uberyoke, then a serial number is required, otherwise leave blank unless it is desired to change the serial number	XXXXXXXXX
	Path for Firmware		Blank
	CCSLoad Directory	Specifies the location the firmware loading software	C:\program files (x86)\picc
	Program Device	Select which device to program	Uberyoke HCU Testset
	Start	Starts the program	n/a
	Errors and Warnings	Shows the values associated with the firmware If an error occurred while talking to hardware, these error windows will indicate the error	Green/blank

10.4.3 Outputs/indicators

	Indicator	Description	Expected Output
	COMM Settings	MSBB communication	(See 10.2 above)
	Command Prompt Output	Shows the all the information generated from the test	n/a
	Standard Error	Shows any errors generated by the third party programs	Blank
	Errors and Warnings	Shows the values associated with the firmware If an error occurred while talking to hardware, these error windows will indicate the error	Green/blank

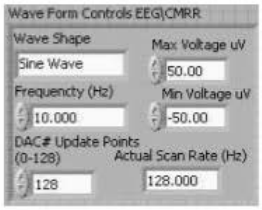
10.5 Master Control Panel

10.5.1 Purpose – To provide control of all the switches, inputs, and outputs of the MSBB. This is the lowest user level control interface for the Testset. This panel has been designed with a pilot/co-pilot model, in that the Testset can be controlled from either this panel or the HCU Console.



10.5.2 Inputs/controls

Table 9

Cluster	Control Name	Description	Default Setting	Switch #
COMM	COMM settings	MSBB communication	(See 10.2 above)	n/a
Waveform controls EEG/CMRR 				n/a
	Wave Shape	Controls the shape of the waveform	Sine Wave Triangle Ramp Flat	n/a
	Frequency (Hz)	Controls the frequency of the waveform	10 (1-100)	n/a
	DAC# Update Points (0-128)	Controls how many points are used to create a single cycle of the waveform	128 (50-128)	n/a
	Max Voltage µV		50 (-399 - 400)	n/a

	Min Voltage µV		-50 (-400-399)	n/a
	Actual Scan Rate	Displays the frequency at which the DAQ is changing the value of the output	N/A (output only)	n/a
Biosig Control 				
Bump Control	Bump Gen	Turns on/off artifact "bump" capability	Off/dull green	LV 30
	Bump Lvl	Controls the amplitude of the bump	High level/dull green	LV 31
	Bump Polarity	Controls the polarity of the bump	POS/dull green	LV 32
	Bump and Offset Controls	Controls the bump and offset for each of the individual channels	Off/dull green	LV 33-39
Signal Control	CMRR	Switches the output signal to CMRR	Off/dull green	LV 8
	Signal switches	Turns on/off the EEG or CMRR signal	On/bright green	LV 1-7
	Offset	Turns on/off a preset offset	Off/dull green	LV 9
	Offset polarity	Switches the polarity of the offset	Off/dull green	LV 10
Impedance	Impedance switches	Controls the input impedance of the signal	20K (0.5k, 20k,56k,76k)	LV 11-LV29
Connection options	HCU Connection Control	Controls data lines	HCU top <-> HCU–bot DAQ <-> HCU-BOT HCU top <-> DAQ	LV 40,41
	Yoke Connection Control	Switches the Uberyoke	DAQ <-> YOKE	LV42

		control from MSBB to HCU	HCU <-> YOKE	
	Programmer Connection	Controls whether the programmer is connected to the Uberyoke or HCU	Program HCU (Program Uberyoke)	LV 43
	Enable HCU Battery Charge	Charges the HCU battery, (requires HCU top to bottom pwr)	Off/dull green	LV 44
	Enable MSBB to HCU power	Powers the HCU directly from the MSBB	Off/dull green	LV 45
	Enable HCU Top to Bottom Power	Connects the HCU top and HCU bottom power lines	Off/dull green	LV 46
	Xpander rst	Resets the port expanders	Off/dull green	LV 47
	Loopback Enable	Loops back the CAL Tone signal into the Uberyoke	Off/dull green	LV 48
	LCD Enable	Enables MSBB control contrast of the LCD	Off/dull green	LV 49
	Current monitor	Switches on/off the current monitor	Off/dull green	n/a
Free Controls	Display EEG	Engages the EEG display	ON/bright green	n/a
	Flush UART	Resets the UART buffer	Off/dull green	n/a
	Create log file	At the test complete stores the waveform to a file	Off/dull green	n/a
UART	Send Command MSBB	Select commands to send to the MSBB	Off/dull green	n/a
	Send Command Uberyoke	Select commands to send to the Uberyoke	Off/dull green	n/a

Errors and warnings			Green/blank	n/a

10.5.3 Output/indicators

Table 10

	Indicator	Description	Expected Output
	COMM Settings		(See 10.2 above)
	Errors and Warnings		
	EEG Display	Display's the output from the Uberyoke	
	Errors and Warnings	Shows the values associated with the firmware If an error occurred while talking to hardware, these error windows will indicate the error	Green/blank

10.6 Initialize Testset Panel

10.6.1 Purpose - The purpose of this panel is to return the Testset to an initial known state which is necessary every time the MSBB is turned on or reset. It is also to be used after a factory reset to restore custom defaults. It can be used at anytime, however, any tests in progress will have to be restarted. It is recommended to use this function first if the system becomes unstable, or acts unpredictably.

10.6.2 Inputs/controls

Table 11

	Control	Description	State(s)
	COMM	MSBB communication	(See 10.2 above)
	Reset Labjack	Soft reset of the Labjack	Off/dull green
	Set Labjack Custom	Sets the defaults on a new Labjack, or after a	Off/dull green

	Defaults	factory reset or new firmware install	

10.6.3 Output/indicators

Table 12

	Outputs	Expected Output	Description
	Xpander Values sent correctly	Bright green	Handshaking with the port expanders, verifies robust communication and functional hardware
	Status	Blinking yellow or bright green	Lets the user know if the VI is running or completed
	Labjack firmware	See Labjack documentation	Contains information about the Labjack firmware
	Errors and Warnings	Green/blank	Shows the values associated with the firmware If an error occurred while talking to hardware, these error windows will indicate the error

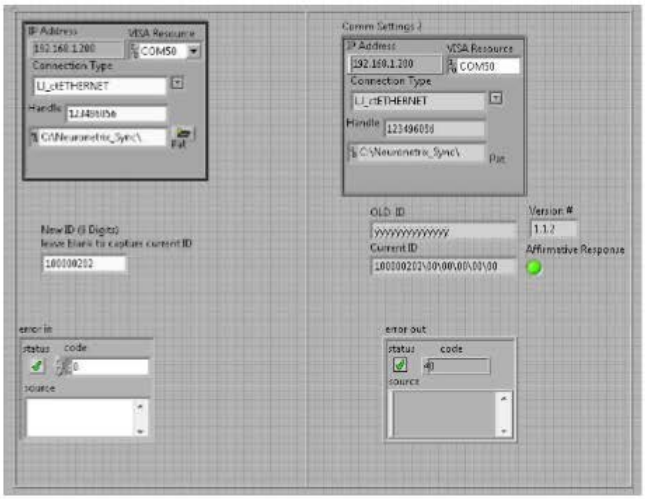
10.6.4 General Instructions - To initialize the MSBB

- Set the COMM settings
- Run the VI

10.6.5 Special Instructions – Execute to initialize the MSBB. To perform a soft reset (remote), activate the reset switch and execute. To reset the custom defaults, activate the "Set Custom Defaults" and execute. A reset may be required after this.

10.7 Load Serial Number Panel

10.7.1 Purpose – To retrieve the current serial number and version number, and/or load a new serial number into the Uberyoke via the Testset's UART.



10.7.2 Input/controls

Table 13

	Control	Description	State(s)
	COMM Settings	MSBB communication	(See 10.2 above)
	New ID	A 9 digit serial number, only used when setting a new value	XXXXXXXXX
	Errors and Warnings	Shows the values associated with the firmware If an error occurred while talking to hardware, these error windows will indicate the error	Green/blank

10.7.3 Output/Indicators

Table 14

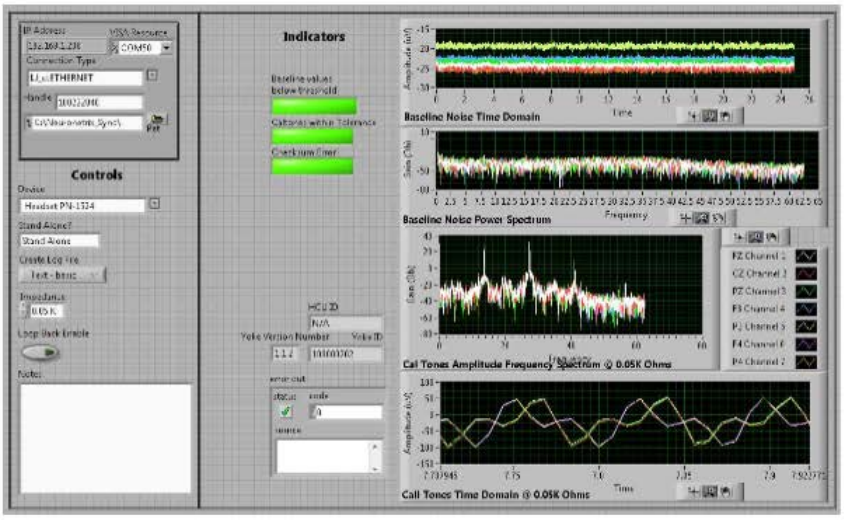
	Indicator	Description	Expected Output
	COMM	MSBB communication	(see above)
	Current ID	ID that is currently stored in the Uberyoke	XXXXXXXXX
	Version #	Version number of Uberyoke	X.X.X
	Old ID	ID that was in Uberyoke before new ID was installed. This indicator is	XXXXXXXXX

		only populated when the serial number is changed	
	Affirmative Response	The indicator will glow bright green if the new ID indicator matches the control	Bright green
	Errors and Warnings	Shows the values associated with the firmware If an error occurred while talking to hardware, these error windows will indicate the error	Green/blank

10.7.4 Special instructions – If a number is written in the NEW ID control, then when the VI is run, it will be written to the Uberyoke, if left blank if will retrieve the current serial number from the Uberyoke.

10.8 Cal Tones, Noise, and Loopback Test Panel

10.8.1 Overview – This panel has multiple purposes, it tests the CAL Tones and baseline noise and can activate the loop back circuit to test an Uberyoke without Electrode Strings.



10.8.2 Input/options

Table 15

	Controls	Description	State(s)
	COMM	MSBB communication	(See 10.2 above)
	Notes		Blank
	Impedance	Sets the impedance for all channels	0.05k
	Loop back enable	Allows the CAL Tone to be looped back into one of the signal paths	False/dull green
	Stand alone?	Used when test is run by itself or as a subVI in a larger program	Normal
	Create log file	Creates a log of the test, including pictures and text	None Text – basic
	Configuration	Selects the current configuration of the Testset	Configuration 1-13

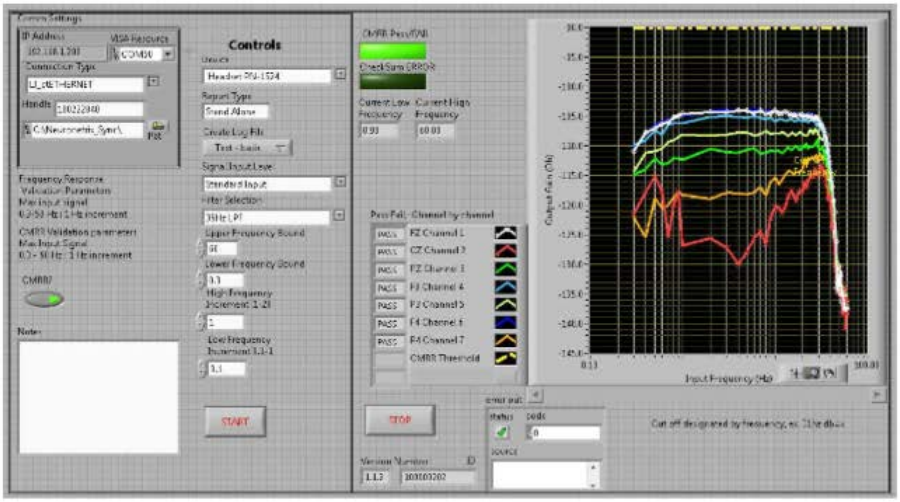
10.8.3 Output/indicators

	Indicator	Description	Expected Output
	Values sent correctly	Green	Monitors xpander values, determines if switches were set properly
	Baseline values below threshold	Green	Indicates if the noise level is below threshold
	CAL Tones Within Tolerance	Green	Indicates if amplitude and frequency of the CAL Tones are correct
	Checksum error	Green	Indicates that no communication interruptions happened during data collection
	Baseline noise time domain	(see image above)	Shows the noise in the time domain
	Baseline noise power spectrum	(see image above)	Shows the noise power spectrum
	CAL Tones amplitude frequency spectrum	(see image above)	Shows the CAL Tones' spectrum of frequencies
	CAL Tones time domain	(see image above)	Shows the CAL Tones time domain
	Errors and warnings	Green/blank	Shows the values associated with the

			firmware If an error occurred while talking to hardware, these error windows will indicate the error

10.9 CMRR Panel

10.9.1 Overview – This panel is used to test the common mode rejection ratio or CMRR. It activates the CMRR switch and injects a common signal into all electrodes (including the common) then compares the input signal to the output signal. The ratio of the output and input represent the amount of common noise the system can reject. This VI works by holding the output amplitude constant and varying the frequency, to test the CMRR at different frequencies.



10.9.2 Input/Controls

Table 16

	Control	Description	Default State
	COMM	MSBB communication	(See 10.2 above)
	Configuration	Selects the current configuration of the Testset Changes what is in the report and possibly some settings	Headset PN-1524
	Report type	Determines the type of report generated, some lines are omitted, others	Normal Stand alone

		are added depending on what test type is selected.	Master test
	Create log file	Creates a log of the test, including pictures and text	None Text - basic
	Signal input level	Changes the amplitude of the input to presets, depending on the test type	Standard Input Max Signal Input
	Filter selection	Selects the low pass filter cutoff from presets	35 Hz LPF 70 Hz LPF
	Upper frequency bound	Selects the highest frequency to be tested	50 (1-62) Integers
	Lower frequency bound	Selects the lowest frequency to be tested	0.3 (0.1-0.9)
	High frequency increment 0.1 – 20	The rate at which the upper frequencies (1 to infinity) change.	1 1-20
	Low frequency increment	The rate at which the lower frequency's (0.1 to 1) change	0.1 (0.1-0.9)
	Notes	Store information about the test being performed that will be printed in the test report	Blank
	START	Press to start test	Pressed, unpressed
	STOP	Press to stop at anytime	Pressed, unpressed
	Errors and Warnings	Shows the values associated with the firmware If an error occurred while talking to hardware, these error windows will indicate the error	Green/blank

10.9.3 Output/Indicators

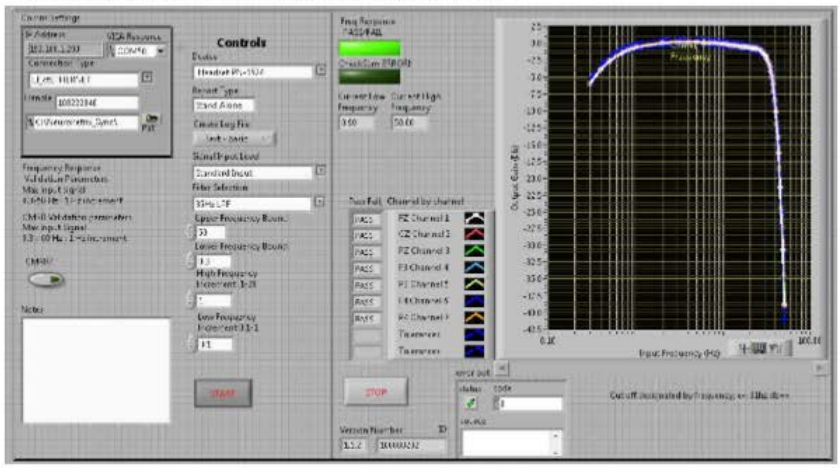
Table 17

	Indicator	Description	Expected Output
	Current low frequency	Gives the present frequency being tested between 0 and 1	0.0
	Current high frequency	Gives the present frequency being tested between 1 and infinity	0.0
	ID	Serial number of	XXXXXXXXX

		Uberyoke	
	Version number	Uberyoke firmware version	X.X.X
	Freq response pass/fail	Indicates whether the test passed or failed	Bright Green
	Checksum error	Indicates whether the communication was robust during the test	Bright Green
	Errors and Warnings	Shows the values associated with the firmware If an error occurred while talking to hardware, these error windows will indicate the error	Green/blank

10.10 Frequency Response

10.10.1 Purpose - The Frequency Response VI determines the voltage amplitude linearity through the amplifiers and filters over a range of frequencies and determines if the LPF is properly rejecting higher frequencies. The COGNISION™ system is specified to have a bandwidth from 0.45 Hz to 33 Hz, denoted by the -3 dB rolloff. This VI works by setting all EEG channels to a single signal amplitude and then increasing the frequency via a sweep function from a lower bound to an upper bound by a predetermined increment. E.g. if the settings were 3, 20, 1 respectively then the frequency response would input a signal initially of 3 Hz, increment that frequency by a value of 1 each data collection period, and then terminate once the frequency reached 20.



10.10.2 Inputs/Controls

Table 18

	Control	Description	State(s)
	COMM	MSBB communication	(See 10.2 above)
	Configuration	Selects the current configuration of the Testset Changes what is in the report and possibly some settings	
	Report type	Determines the type of report generated, some lines are omitted, others are added depending on what test type is selected.	Normal, Stand Alone, Master test
	Create log file	Creates a log of the test, including pictures and text	None, Text - basic
	Signal input level	Changes the amplitude of the input to presets, depending on the tested type	Standard Input Max Signal Input
	Filter Selection	Selects the low pass filter cutoff from presets	35 Hz LPF 70 Hz LPF
	Upper frequency bound	Selects the highest frequency to be test	50 (1-62) Integers
	Lower frequency bound	Selects the lowest frequency to be tested	0.3 (0.1-0.9)
	High frequency increment	The rate at which the upper frequencies (1 to infinity) change.	1 1-20
	Low frequency increment	The rate at which the lower frequency's (0.1 to 1) change	0.1 (0.1-0.9)
	Notes	Store information about the test being performed that will be printed in the test report	Blank
	START	Press to start test	Pressed, unpressed
	Errors and Warnings	Shows the values associated with the firmware If an error occurred while talking to hardware, these	Green/blank

		error windows will indicate the error	

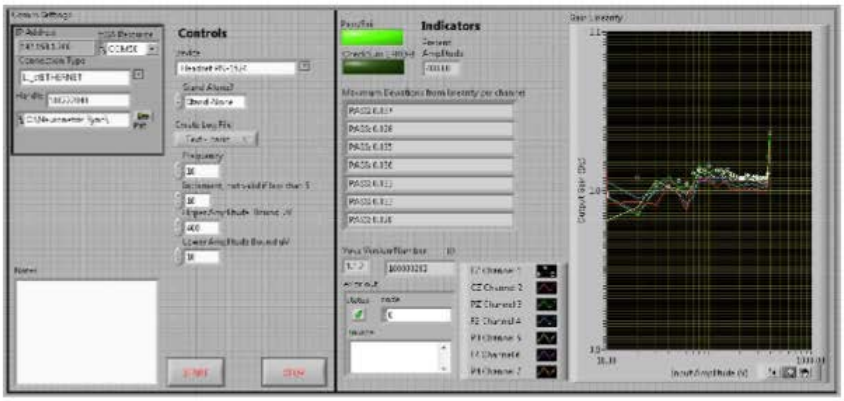
10.10.3 Outputs/Indicators

Table 19

	Indicator	Description	Expected Output
	COMM	MSBB communication	(see above)
	Current low frequency	Gives the present frequency being tested between 0 and 1	0.0
	Current high frequency	Gives the present frequency being tested between 1 and infinity	0.0
	ID	Serial number of Uberyoke	XXXXXXXXX
	Version number	Uberyoke firmware version	0.0.0
	Freq response pass/fail	Indicates if the test passed	Bright Green
	Checksum error	Indicates whether communication was robust during the test	Bright Green
	Errors and Warnings	Shows the values associated with the firmware If an error occurred while talking to hardware, these error windows will indicate the error	Green/blank

10.11 Gain Linearity

10.11.1 Purpose – Measures the linearity of the signal as a ratio of the input/output of an Uberyoke. The closer the value is to one, unity, the more linear the device. An ideal device would produce a straight line where all values are equal to one for different amplitudes.



10.11.2 Input/controls

Table 20

	Control	Description	State(s)
	COMM	MSBB communication	(See 10.2 above)
	Configuration	Selects the current configuration of the Testset Changes what is in the report and possibly some settings	Uberyoke PN-1509 Headset PN-1524
	Stand alone?	Determines the type of report generated, some lines are omitted others added depending on what test type is selected.	Normal, Stand Alone, Master Test
	Create log file	Creates a log of the test, including pictures and text	None, Text – Basic,
	Frequency	Sets the frequency the test is performed at	10, 1-100
	Increment, not valid if less than 5	Sets the frequency increment	10, 5-50
	Upper amplitude bound (uV)	The high amplitude to be tested	400, -390-400
	Lower amplitude bound (uV)	The lowest amplitude to be tested	-390, 400-390
	Notes	Store information about the test being performed that will be printed in the test report	Blank

	START	Press to start test	Pressed, unpressed
	STOP	Push to stop the test	Pressed, unpressed

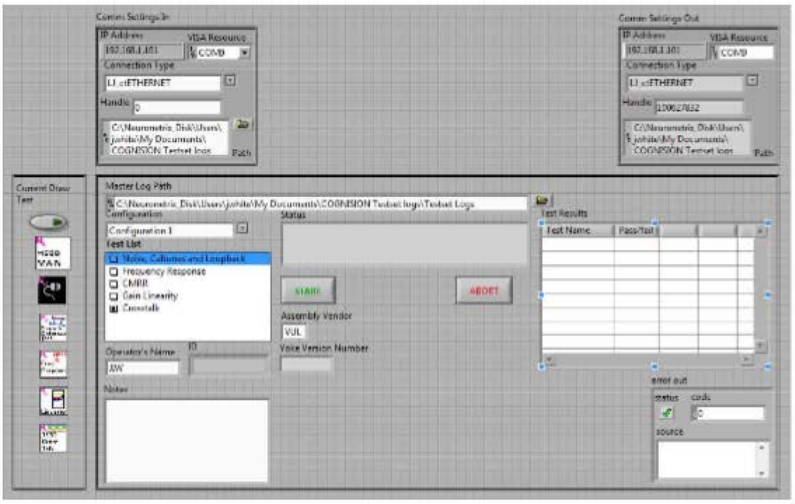
10.11.3 Output/indicators

Table 21

	Indicator	Description	Expected Output
	Present amplitude	Displays the amplitude currently being tested	0.00
	ID	Serial number of Uberyoke	XXXXXXXXX
	Gain Linearity Chart	Displays the gain linearity results graphically	Displays test results
	Pass/fail		Bright green
	Checksum error!	Indicates whether communication was robust during the test	Bright Green
	Linearity per channel	Pass or fail with the value of the maximum deviation from linearity	Pass : 0.0XX
	Errors and Warnings	Shows the values associated with the firmware If an error occurred while talking to hardware, these error windows will indicate the error	Green/blank

10.12 Master Test

10.12.1 Purpose – An automated top level test suite that provides the ability to select which tests to perform and generates a pdf report.



10.12.2 Input/controls

Table 22

	Controls	Description	State(s)
	COMM Settings	MSBB communication	(See 10.2 above)
	Master log path	Gives the location	C:\....\....
	Frequency Response Popup	Opens the front panel for the Frequency Response test	Pressed, unpressed
	Current Draw Test	Engages the test to check the current levels right after initializes the test set.	Pressed, unpressed
	CMRR Popup	Opens the front panel for the CMRR test	Pressed, unpressed
	GAIN Linearity Popup	Opens the front panel for the GAIN Linearity test	Pressed, unpressed
	Crosstalk Popup	Opens the Crosstalk	Pressed, unpressed
	Configuration	Selects the current configuration of the Testset Changes what is in the report and possibly some settings	Uberyoke PN-1509 Headset PN-1524
	Test List	Allows the user to select different tests	Any combination is available

	Operator's name	Name of the person performing the test, will be added to the test report	<String>
	Notes	Any test notes, will be added to the test report	<String>
	START	Push to start test	Pressed, unpressed
	STOP	Push to stop the test	Pressed, unpressed

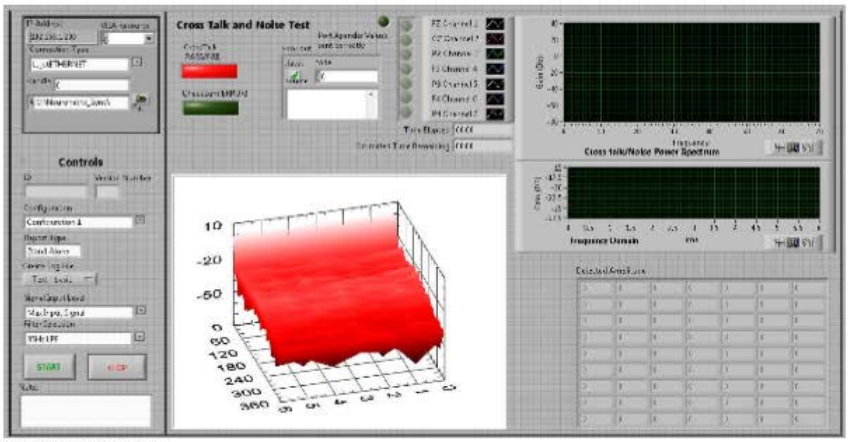
10.12.3 Output/indicators

Table 23

	Indicator	Description	Expected Output
	ID	Uberyoke serial number	XXXXXXXXX
	Status	Gives the status of the test, what test is being run, when it's finished	Examples: Press Start, Finished, (name of test in progress)
	Test results	A table with the test name and the status of the test upon completion	Chart with the test name and a PASS/FAIL designation
	Errors and warnings	Shows the values associated with the firmware If an error occurred while talking to hardware, these error windows will indicate the error	Green/blank

10.13 Crosstalk test

10.13.1 Purpose – To determine the amplitude of crosstalk between the 7 channels of the Headset, by injecting a single frequency into each channel 1 at a time and measuring the amplitude of that frequency in other channels.



10.13.1.1 Input/controls

	Controls	Description	State(s)
	COMM Settings	MSBB communication	(See 10.2 above)
	Master log path	Gives the location	C:\....\....
	Configuration	Selects the current configuration of the Testset Changes what is in the report and possibly some settings	Uberyoke PN-1509 Headset PN-1524
	Stand alone?	Determines the type of report generated, some lines are omitted others added depending on what test type is selected.	Normal, Stand Alone, Master Test
	Create log file	Creates a log of the test, including pictures and text	None, Text – Basic,
	Signal input level	Changes the amplitude of the input to presets, depending on the tested type	Standard Input Max Signal Input
	Filter Selection	Selects the low pass filter cutoff from presets	35 Hz LPF 70 Hz LPF

10.13.1.2 Output/indicators

	Indicator	Description	Expected Output
	ID	Uberyoke serial number	XXXXXXXXX
	Status	Gives the status of the test, what test is being run, when it's finished	Examples: Press Start, Finished, (name of test in progress)
	Test results	A table with the test name and the status of the test upon completion	Chart with the test name and a PASS/FAIL designation
	Errors and warnings	Shows the values associated with the firmware If an error occurred while talking to hardware, these error windows will indicate the error	Green/blank

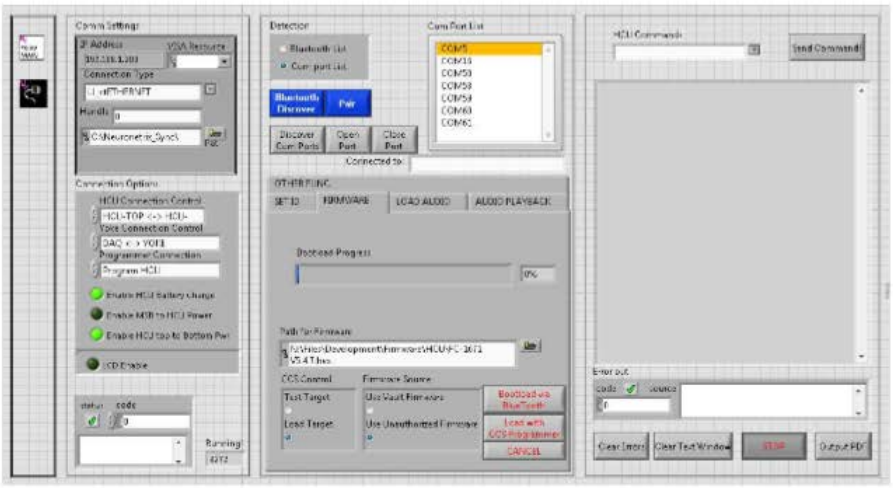
10.14 HCU Console

10.14.1 Purpose – A top level control panel for the various functions of the HCU. This panel has been designed with a pilot/co-pilot model, in that the Testset can be controlled from either this panel or the Master Control Panel simultaneously.

10.14.2 Pairing and connecting instructions –

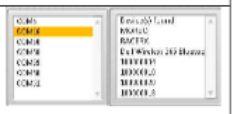
1. Ensure power is going to the HCU and that it is turned on.
2. If the device is already paired, then skip past the pairing to connecting
3. DISCOVERING: Click the Bluetooth Discover
4. Once the discover list has been populated, click on the desired device
5. Allow the unit to pair
6. CONNECTING: Click on Discover Com Ports
7. Click on the port of the desired device
8. Click Open Port

Note: If another device is desired than the one connected to, first click close port then repeat these instructions for the new device



10.14.2.1 Input/controls

	Controls	Description	State(s)
	Controls	Description	State(s)
	COMM Settings	MSBB communication	(See 10.2 above)
Popup Buttons	MSBB Control	Master Control Panel button for launching the master control panel	
Connection Options			
	HCU Connection Control	Controls data lines	HCU top <-> HCU–bot DAQ <-> HCU-BOT HCU top <-> DAQ
	Yoke Connection Control	Switches the Uberyoke control from MSBB to HCU	DAQ <-> YOKE HCU <-> YOKE
	Programmer Connection	Controls whether the programmer is connected to the Uberyoke or HCU	Program HCU (Program Uberyoke)
	Enable HCU Battery Charge	Charges the HCU battery, (requires HCU top to bottom pwr)	Off-dull/green
	Enable MSBB to HCU power	Powers the HCU directly from the MSBB	Off-dull/green
	Enable HCU Top to Bottom Power	Connects the HCU top and HCU bottom power lines	Off-dull /green

	LCD Enable	Enables MSBB control contrast of the LCD	Off-dull green
HCU Connection Options			
	Bluetooth Discover	Displays list of Bluetooth devices within range of the Bluetooth radio	Unpressed/pressed
	Pair	Pairs with the selected Bluetooth device	Unpressed/pressed
	Discover Com Ports	Displays list of all	Unpressed/pressed
	Open Port	Opens a connection to the selected port	Unpressed/pressed
	Close Port	Closes the currently open port	Unpressed/pressed
	ComPort/Bluetooth listbox	Displays either the list of Bluetooth devices discovered, or the list of comports available on the computer	
Function Tab			
Set ID	Check Number	Checks to see if there are enough digits in the number, and that it is all numbers (no letters)	N/A
	Load HCU ID	Button to execute the loading of the HCU's new SN	Unpressed/pressed
	Load Yoke ID	Button to execute the loading of the Yoke's new SN	Unpressed/pressed
	New HCU ID:	9 digit integer value for the HCU SN	9 Digit string input
	New Yoke ID:	9 digit integer value for the Yoke's SN	9 Digit string Input
Firmware Tab			
	Path for Firmware	Describes the path to the alternative firmware	**BLANK**/path txt
	CCS Control	Directs the CSS to either test the target chip, or load the firmware to the target chip	Test target/ load target
	Firmware Source	Directs the firmware function to retrieve the firmware from either the vault or from the user given path	Use vault firmware/ use unauthorized firmware

	Bootload via Bluetooth	Use the Bluetooth communication protocol to load the firmware	Unpressed/pressed
	Load with CCS Programmer	Use the CCS programmer (via USB) to load the firmware	Unpressed/pressed
	Cancel	Cancel the firmware loading process	Unpressed/pressed
Load Audio			
	# of Slots to load	Select how many audio files are going to be loaded/how many slots will be loaded	**1** Slider from 1 to 6
	Audio Type	Directs the audio to be loaded either as audio tones or as audiometry tones	**Audio**/audiometry
	Audio File Path	The path for where the function should find the audio file	Blank, File path
	Load	Executes the load audio file	Unpressed/pressed
	Cancel	Cancels the audio loading function	Unpressed/pressed
Audio Playback			
	Audio Type	Selects whether to play audio tones or audiometry tones	**Audio**/Audiometry
	Audio Slots	Selects which slot to play from, 1-7	**0** 0-6
	Device ID	The device ID is an integer value set by the operating system, each sound device on the computer has a different number.	**0**
	Milliseconds	Part of the repeat playback functionality, this number is the time delay in ms that the console waits before sending the command to play a tone again.	**2000 ms integer increment 0-inf**
	dB to Play	Selects how loud to play the tones	**30db** slider 0-120db
	Sound Capture	Selects whether the playback should be	**Off** dull green/Bright green

		captured and dispalyed	
	Repeat	Checkbox for engaging the repeat function. This function will repeat the selected tone when play is pressed at the designated time interval set by milleseconds	
	Play	Plays the currently selected tone at the designated amplitude	
	Stop	Stops playing tones when the repeat function is pressed.	
Other Func.			
	Impedance Values	Sets the impedance values for the test set for the different channels, if the user wish's to change all values at the same time, then use the All channel	0,1,2,3 Corresponding to 0.5k, 20k, 56k, 76k
	Initiate Impedance Test	Send the command to the HCU to start the Impedance test protocol, then	Unpressed/pressed
	Cancel	Terminates the other func. Process	Unpressed/pressed
	HCU Commands	List of all the commands available to send to the HCU. Select the command then press send command	**Blank** Combo box
	Send Command!	Sends the selected HCU command.	Unpressed/pressed
	Clear Errors	Clears any errors that are being displayed in the Error out indicator	Unpressed/pressed
	Clear Text Window	Clears any txt displayed in the DSS, impedance, or local echo	Unpressed/pressed
	Stop	Stops the program	Unpressed/ pressed
	Output PDF	Future use, will generate a pdf of the local echo	Unpressed/pressed
Launcher buttons			
	Master Control Panel	Launches the master control panel and runs it	Unpressed/pressed

	Terminal Window	Launches the terminal window	Unpressed/pressed
	Controls	Description	State(s)

	Indicator	Description	Expected Output
	Running!	A counter that increments as long as the program is looping	A positive inteteger
	Com Port/Bluetooth Listbox	A interactive indicator that displays either the Bluetooth devices or comports	Bluetooth devices or com ports depending on what is selected
	Connected to:	A string output that displays when the port is connected to a device	ASTR(portnumber)::
Firmware Tab	Bootload Progress	A progress bar	Sliding bar, full when finished
Load Audio Tab	Audio Loading progress	A progress bar for the total audio data loaded into the HCU	Sliding bar, full when finished
Audio Playback tab			
	Playing	Indicator to show when the playback is active	Bright green light when active, dull green when off
	Audio Error	Error during audio capture	Lit red when error occurs
	Audiometer	Display the sound pressure of the sound captured during the playback	Sliding needles which demonstrate the recorded sound pressure
	Sound capture graph	Displays the graph of the sound captured during the playback	Shows the sound capture wave form
Other Func. Tab			
	Impedance test window	Displays impedance values after impedance test	Fz Cz Pz F3 P3 F4 P4 M1 M2 -- -- -- -- -- -- -- -- -- 20 01 01 19 19 20 19 17 23
	Device Status Stream Window	Displays the parsed values from the DSS command issued to the HCU	
	Local Echo Window		

	Error Out		

10.15 COGNISION™ Testset Launcher

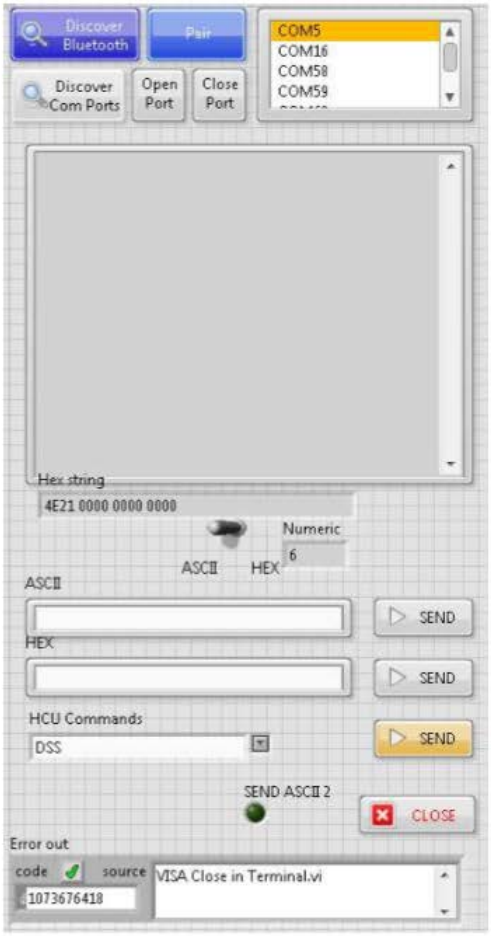
10.15.1 Purpose – The topmost level program in the COGNISION™ Testset suite. It has multiple tabs for running or launching any of the tests for the Testset.

	Controls	Description	State(s)
	Tab Control	Allows the selection of the different test or functions	**Master Test**/Selected Tab
	Run Button	Each tab has a run button associated with it that will execute that particular test	Unpressed/Pressed
Macros Tab			Unpressed/Pressed
	Initialize Testset button	Launches the testset initialization VI	Unpressed/Pressed
	Terminal Launcher	Launches the Terminal VI	Unpressed/Pressed
	Initalize for RFI	Launches the Macro that	Unpressed/Pressed

	frequency Interfrence testing	reconfigures the testset for the RFI test	
	Global Stop	Stop All programs	Unpressed/Pressed

10.16 Terminal

10.16.1 Purpose – Serves as a terminal program for connecting to a serial port and sending or receiving commands. (See HCU Console for instructions on connecting and disconnecting from a device)



	Controls	Description	State(s)

HCU Connection Options			
	Bluetooth Discover	Displays list of Bluetooth devices within range of the bluetooth radio	Unpressed/pressed
	Pair	Pairs with the selected Bluetooth device	Unpressed/pressed
	Discover Com Ports	Displays list of all	Unpressed/pressed
	Open Port	Opens a connection to the selected port	Unpressed/pressed
	Close Port	Closes the currently open port	Unpressed/pressed
	ComPort/Bluetooth listbox	Displays either the list of Bluetooth devices discovered, or the list of comports available on the computer	
	ASCII vs HEX	Changes the echo from ASCII to HEX	**ASCII**/HEX
	ASCII	ASCII command window, ASCII commands typed here can be sent to the terminal device	**Blank**, text
	Send ASCII	Sends the ASCII command	Unpressed/pressed
	HEX	HEX command window, HEX commands typed here can be sent to the device	**Blank**, HEX numeric
	Send HEX	Sends the HEX command	Unpressed/pressed
	HCU Commands	All available HCU commands are contained here, the command that is to be sent can be selected here	**Blank**, HCU COMMAND txt
	Send HCU command	Send's the HCU command	Unpressed/pressed
	Close	Stops the program, closes the window	Unpressed/pressed

	Indicator	Description	Expected Output
	Terminal Window	Displays the information received from the terminal device, and the	

		commands sent out to it	
	Hex String	Hex version of whatever command is sent	4 group hex number
	Running!	Indicates to the user if the program is running or halted	Incrementing integers starts at 0 at program start
	Error Out		

11 DETAILED TEST PROTOCOLS

- For any test performed on a new unit that has not previously been tested, test #1 a power consumption test, is required to ensure that there are no harmful shorts present.
- For all tests that include Electrode Strings or a Headset, test #7 the Connectivity Test is required to ensure robust connections have been made at the contact points.

11.1 Configuration 1

11.1.1 Automated test procedure

- Open Master Test.exe
- Set the COMM settings: IP Address, VISA Resource, and Connection Type
- Check the Master log Path to ensure the path is pointed at the correct folder
- Set the configuration control to configuration 1
- Select the tests:
    - #8,6 Noise, CAL Tones and Loopback
    - #18 Frequency Response
    - #14 CMRR
    - #17 Gain Linearity
- Fill in the operators name (If this step is forgotten the program will request it later)
- Fill in any notes that pertain to this test that should be included in the report
- Press Start
- See Section 12 below for results

11.2 Configuration 2

11.2.1 Automated test procedure

- Open Master Test.exe
- Set the COMM settings: IP Address, VISA Resource, and Connection Type
- Check the Master log Path to ensure the path is pointed at the correct folder
- Set the configuration control to 2
- Select the tests:
    - #8,6 Noise, CAL Tones and Loopback
    - #18 Frequency Response
    - #14 CMRR
    - #17 Gain Linearity
- Fill in the operators name (If this step is forgotten the program will request it later)
- Fill in any notes that pertain to this test that should be included in the report
- Press Start
- See Section 12 below for results

11.3 Configuration 10

11.3.1 #7 Check for Connectivity

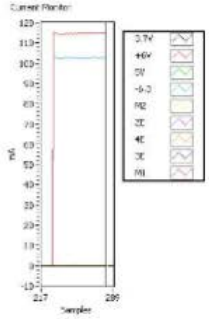
11.3.2 Automated test procedure

- Open Master Test.exe

- Set the COMM settings: IP Address, VISA Resource, and Connection Type
- Check the Master Log Path to ensure the path is pointed at the correct folder
- Set the configuration control to 10
- Select the tests:
    - #8,6 Noise, CAL Tones and Loopback
    - #18 Frequency Response
    - #14 CMRR
    - #17 Gain Linearity
- Fill in the operators name (If this step is forgotten the program will request it later)
- Fill in any notes that pertain to this test that should be included in the report
- Press Start
- See Section 12 below for results

12 TEST RESULTS

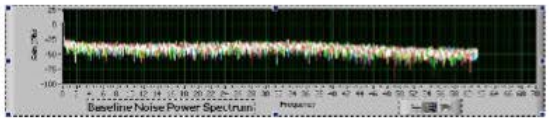
12.1 Power Consumption test results for Uberyoke PN-1509



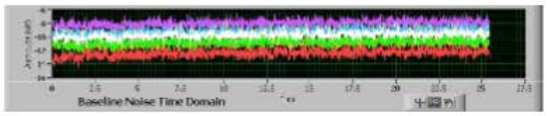
3.7V	50 mA @ steady state no activity (with spikes to 90 mA from bluetooth)
+6V	115-120 mA (switches disabled) 155-160 mA (all switches enabled)
5V	50-461 mA depending on battery state
-6.3V	102-105 mA
M2	1.8-2.7 mA
ZE	6.5-7.5mA
4E	4.3-5 mA
3E	4.3-5 mA
M1	1.8-2.7 mA

12.2 Baseline Noise

12.2.1 Baseline Power spectrum should all be flat and less than -20 dB

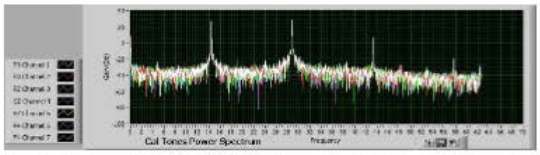


12.2.2 Baseline time domain should be less than 5uV pk-pk and <1 µV

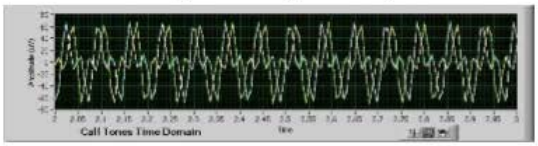


12.3 CAL Tones and Loopback

12.3.1 CAL Tones power spectrum should contain three peaks at 13.9, 28.8 and a third around 45.

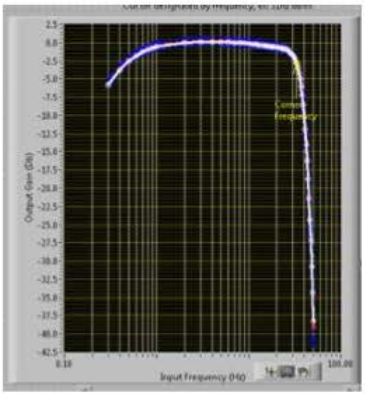


12.3.2 CAL Tones Time Domain should have two signals 180 degrees out of phase with each other.



12.4 Frequency Response

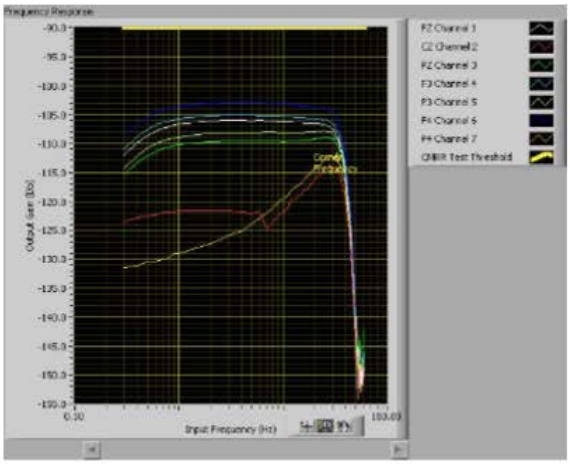
12.4.1 All signals should have the same values, and fall between the dark blue lines



12.5 CMRR

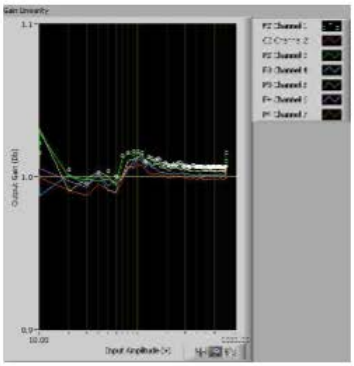
12.5.1 Open CMRR & Frequency Response VI

12.5.2 All values should be below -90 dB



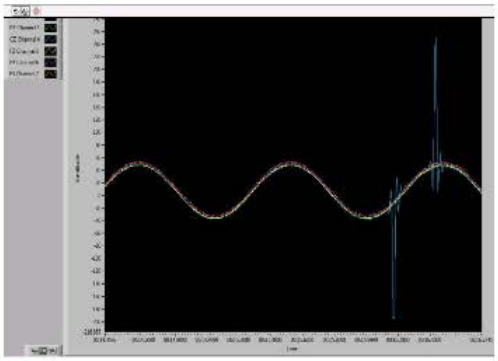
12.6 Gain Linearity

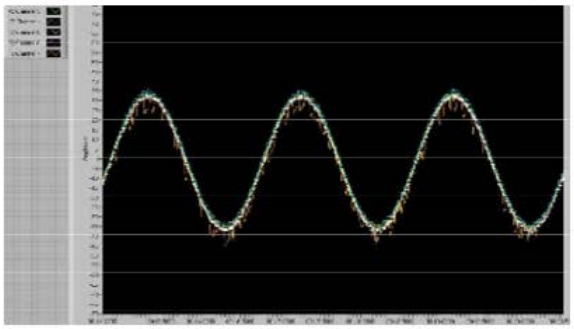
The gain linearity graph would optimally be a straight line with the being equal to 1.0 across the entire spectrum of voltages tested. The threshold is set so all amplitudes greater than 10 mV must have a slope less than 1.05 and greater than 0.95 to pass.

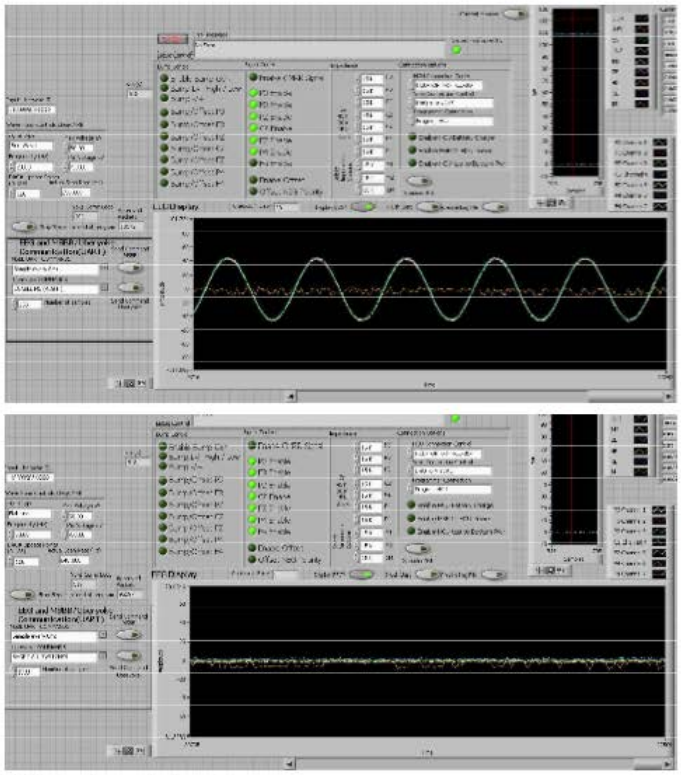


13 FAILURE MODES

13.1 Bad Switch Cap Filter

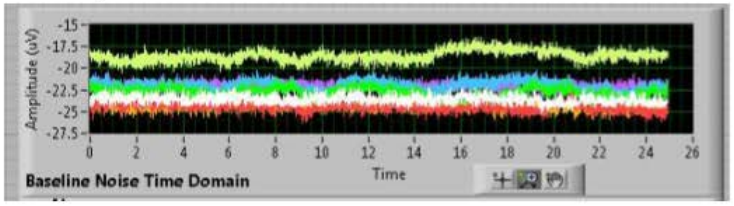






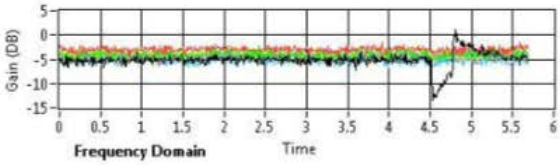
- SOLUTION: Replace switch cap filter

13.2 Uncovered Uberyoke

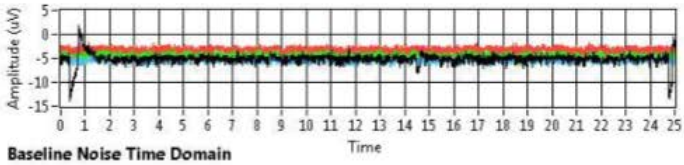


- SOLUTION: cover the Uberyoke

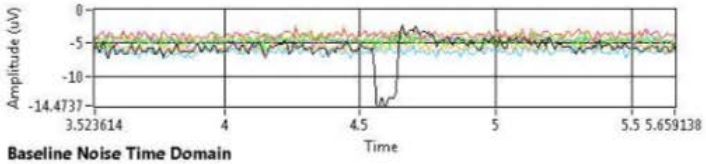
13.3 Popcorn hic-up



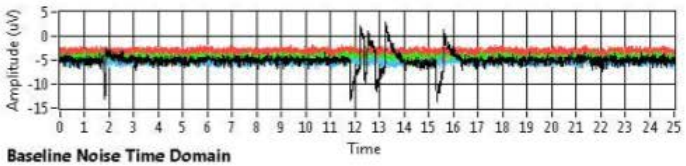
Frequency Domain



Baseline Noise Time Domain



Baseline Noise Time Domain



Baseline Noise Time Domain

14 TEST REPORT VR-1524

VR-1524 Date/Time: 2/20/2012 4:08:00 PM Operator: JIW

****

Test: Headset

Configuration: 10

Serial Number : 100000215

Date/Time: 2/20/2012 4:19:42 PM

Firmware Version: 1.1.2

Duration: 11:41

Status: PASS

****

Tests Performed:

- Current Draw
- Caltones, Noise and Loopback
- Frequency Response
- CMRR
- Gain Linearity
- Crosstalk

Notes:Validation

****

****

Test: Caltones, Noise and Loopback

Date/Time: 2/20/2012 4:09:49 PM

Duration: 01:42

Status: PASS

****

Electrode / Channel

Noise Vpk-pk: < 5 uV

Noise V RMS: < 1 uV

Low Cal Frequency: 13.50 - 14.50 Hz

Low Cal Power: 31.5 - 33.5 dB uV

High Cal Frequency: 27.00 - 28.00 Hz
High Cal Power: 31.5 - 33.5 dB uV

FZ / 1
PASS: 2.913086
PASS: 0.544692
PASS: 13.671886
PASS: 32.733702
PASS: 27.343759
PASS: 32.750293

CZ / 2
PASS: 3.190523
PASS: 0.499263
PASS: 13.671877
PASS: 32.715826
PASS: 27.343757
PASS: 32.667964

PZ / 3
PASS: 3.329241
PASS: 0.527230
PASS: 13.671887
PASS: 32.683206
PASS: 27.343746
PASS: 32.639486

F3 / 4
PASS: 3.190523
PASS: 0.533119
PASS: 13.671874
PASS: 32.659008
PASS: 27.343754
PASS: 32.595108

P3 / 5
PASS: 3.467960

PASS: 0.493493
PASS: 13.671887
PASS: 32.673726
PASS: 27.343774
PASS: 32.609141

F4 / 6
PASS: 2.913086
PASS: 0.520396
PASS: 13.671879
PASS: 32.683702
PASS: 27.343767
PASS: 32.661140

P4 / 7
PASS: 3.329241
PASS: 0.493065
PASS: 13.671882
PASS: 32.740142
PASS: 27.343785
PASS: 32.670850
****

****
Test: Frequency Response
Date/Time: 2/20/2012 4:12:58 PM
Duration: 03:08
Status: PASS
****
Electrode / Channel
Max Deviation: < 0.2*x+0.45 dB @ 0.2-0.4 Hz
Max Deviation: < 0.45 dB @ 0.3-32 Hz
Max Deviation: < 0.15*x+0.45 dB @ 33-50 Hz
Gain @ 33 Hz: -3.418 < x < -2.218 dB
Gain @ 10 Hz: -0.38 < x < 0.52 dB

Gain @ 0.4 Hz: -3.90 < x < -2.70 dB

Gain Passband Values

Variance 1-20 Hz : < 1 dB

FZ / 1

PASS: data within tolerance

PASS: data within tolerance

PASS: data within tolerance

PASS: -2.68

PASS: 0.03

PASS: -3.19

-2.042, -1.359, -0.887, -0.628, -0.451, -0.291, 0.218, 0.320, 0.327, 0.294, 0.243, 0.216, 0.151, 0.100, 0.028, 0.003, -0.059, -0.145, -0.185, -0.238, -0.273, -0.334, -0.363, -0.400, -0.430, -0.505, -0.475, -0.577, -0.633, -0.729, -0.827, -0.944, -1.127, -1.281, -1.560, -1.872, -2.195

PASS: 0.7560

CZ / 2

PASS: data within tolerance

PASS: data within tolerance

PASS: data within tolerance

PASS: -2.66

PASS: 0.05

PASS: -3.33

-2.144, -1.434, -0.907, -0.619, -0.462, -0.294, 0.232, 0.329, 0.340, 0.336, 0.270, 0.226, 0.178, 0.120, 0.049, 0.002, -0.050, -0.102, -0.176, -0.212, -0.291, -0.330, -0.349, -0.382, -0.403, -0.485, -0.538, -0.519, -0.618, -0.720, -0.759, -0.851, -1.056, -1.256, -1.485, -1.742, -2.161

PASS: 0.7421

PZ / 3

PASS: data within tolerance

PASS: data within tolerance

PASS: data within tolerance

PASS: -2.72

PASS: 0.02

PASS: -3.38

-2.184, -1.482, -1.012, -0.693, -0.523, -0.362, 0.190, 0.275, 0.267, 0.264, 0.199, 0.157, 0.097, 0.082, 0.017, -0.039, -0.081, -0.174, -0.211, -0.282, -0.316, -0.413, -0.403, -0.484, -0.521, -0.573, -0.558, -0.621, -0.689, -0.809, -0.827, -0.948, -1.079, -1.241, -1.517, -1.844, -2.230

PASS: 0.7962

F3 / 4

PASS: data within tolerance

PASS: data within tolerance

PASS: data within tolerance

PASS: -2.69

PASS: -0.01

PASS: -3.32

-2.175, -1.457, -0.983, -0.675, -0.511, -0.362, 0.155, 0.241, 0.254, 0.250, 0.212, 0.171, 0.114, 0.061, -0.011, -0.049, -0.118, -0.179, -0.203, -0.329, -0.299, -0.376, -0.405, -0.445, -0.437, -0.495, -0.537, -0.603, -0.627, -0.707, -0.818, -0.900, -1.041, -1.196, -1.512, -1.815, -2.211

PASS: 0.6985

P3 / 5

PASS: data within tolerance

PASS: data within tolerance

PASS: data within tolerance

PASS: -2.70

PASS: 0.06

PASS: -3.39

-2.197, -1.475, -0.995, -0.708, -0.537, -0.339, 0.204, 0.302, 0.323, 0.294, 0.236, 0.209, 0.161, 0.119, 0.061, -0.014, -0.076, -0.151, -0.191, -0.249, -0.332, -0.368, -0.371, -0.437, -0.471, -0.527, -0.574, -0.626, -0.608, -0.763, -0.821, -0.965, -1.146, -1.306, -1.535, -1.830, -2.219

PASS: 0.7937

F4 / 6

PASS: data within tolerance

PASS: data within tolerance

PASS: data within tolerance

PASS: -2.67

PASS: 0.03

PASS: -3.22

-2.086, -1.416, -0.965, -0.666, -0.482, -0.318, 0.199, 0.271, 0.306, 0.293, 0.235, 0.195, 0.141, 0.091, 0.031, -0.009, -0.106, -0.155, -0.180, -0.237, -0.311, -0.372, -0.368, -0.480, -0.494, -0.483, -0.548, -0.592, -0.672, -0.791, -0.810, -0.938, -1.084, -1.209, -1.440, -1.766, -2.179

PASS: 0.8000

P4 / 7

PASS: data within tolerance

PASS: data within tolerance

PASS: data within tolerance

PASS: -2.56

PASS: 0.10

PASS: -3.27

-2.086, -1.388, -0.938, -0.618, -0.437, -0.273, 0.253, 0.347, 0.363, 0.345, 0.305, 0.271, 0.211, 0.170, 0.101, 0.020, -0.014, -0.083, -0.125, -0.190, -0.257, -0.290, -0.308, -0.376, -0.417, -0.470, -0.527, -0.531, -0.607, -0.731, -0.755, -0.873, -1.007, -1.255, -1.429, -1.721, -2.126

PASS: 0.7800

****

****

Test: CMRR

Date/Time: 2/20/2012 4:16:31 PM

Duration: 03:32

Status: PASS

****

Electrode / Channel

Min Attentuation : < 90 dB

CMRR @ 60 HZ : <100 dB

CMRR @ 50 HZ : < 100 dB

FZ / 1

PASS: -99.71

PASS: -150.66

PASS: -139.86

CZ / 2

PASS: -94.57

PASS: -142.59

PASS: -134.01

PZ / 3

PASS: -94.27

PASS: -141.91

PASS: -133.51

F3 / 4
PASS: -103.31
PASS: -151.46
PASS: -139.41

P3 / 5
PASS: -101.92
PASS: -151.69
PASS: -139.87

F4 / 6
PASS: -105.96
PASS: -148.95
PASS: -143.25

P4 / 7
PASS: -104.56
PASS: -146.88
PASS: -142.43
****

****
Test: Gain Linearity
Date/Time: 2/20/2012 4:18:30 PM
Duration: 01:58
Status: PASS
****
Electrode / Channel
Maximum deviation from linearity : < 0.1

FZ / 1
PASS: 0.050

CZ / 2

PASS: 0.032

PZ / 3
PASS: 0.080

F3 / 4
PASS: 0.030

P3 / 5
PASS: 0.032

F4 / 6
PASS: 0.074

P4 / 7
PASS: 0.053
****

****
Test: Crosstalk
Date/Time: 2/20/2012 4:19:40 PM
Duration: 01:10
Status: PASS
****
Electrode / Channel
Minimum Crosstalk >60 db
@ 10hz, 730 mv pk-pk input on driven CH

Driven Electrode / Channel
FZ Crosstalk : >60 dB
CZ Crosstalk : >60 dB
PZ Crosstalk : >60 dB
F3 Crosstalk : >60 dB
P3 Crosstalk : >60 dB
F4 Crosstalk : >60 dB

P4 Crosstalk : >60 dB

FZ Channel 1
Driven
PASS : 68.880158
PASS : 70.731071
PASS : 66.741763
PASS : 72.162827
PASS : 70.982802
PASS : 71.165822

CZ Channel 2
PASS : 71.698031
Driven
PASS : 71.636685
PASS : 64.244081
PASS : 72.619182
PASS : 70.200135
PASS : 71.036055

PZ Channel 3
PASS : 73.454368
PASS : 71.093202
Driven
PASS : 67.378611
PASS : 73.710939
PASS : 71.665873
PASS : 72.532700

F3 Channel 4
PASS : 71.636578
PASS : 71.669383

PASS : 69.734819
Driven
PASS : 70.319606
PASS : 72.211564
PASS : 70.742590

P3 Channel 5
PASS : 71.187832
PASS : 71.571074
PASS : 72.408606
PASS : 65.433839
Driven
PASS : 69.730330
PASS : 71.406858

F4 Channel 6
PASS : 72.491789
PASS : 72.123260
PASS : 69.700249
PASS : 72.727017
PASS : 69.593354
Driven
PASS : 67.199556

P4 Channel 7
PASS : 70.044919
PASS : 70.345440
PASS : 73.113579
PASS : 71.359017
PASS : 71.046375
PASS : 72.629407
Driven

****

15 DEPLOYING HEADSET TEST SYSTEM

15.1 Requirements

- Headset Test System Installer
- Testset executables directory
- Testset
- Computer 32bit with Windows 7™ operating system
- Labjack installer

15.2 Instructions

- Copy the Headset Test system installer to the desired computer
- Run setup and follow instructions
- This step installs the LabVIEW Runtime Engine™ and the VISA™ drivers.
- Copy the labjack installer to the desired computer
- Run setup and follow instructions
- This step installs the labjack drivers

15.3 Copy the Testset Executables directory to the desktop

15.4 Deployment complete

16 REFERENCE DOCUMENTS

16.1 PN-1486 MSBB - PCA

16.2 PS-1554 AUDIOMETRY OVERVIEW AND SYSTEM SPECIFICATION

16.3 PN-1558 HEADSET TEST BOARD - PCA

16.4 EL-1558 HEADSET TEST BOARD EAGLE SCHEMATIC

16.5 PN-1559 HEADSET TEST SETUP

16.6 PS-1560 LABVIEW TESTSET CONTROLLER

16.7 SC-1673 HEADSET TEST SYSTEM

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IX. VITA

Joshua Isaac White is from Louisville, Kentucky and completed a Bachelor of Science degree in Bioengineering at the University of Louisville in 2010. He currently is employed by Neuronetrix as the director of validation and testing. Upon completion of his master's degree he will (hopefully) be continuing his education at UofL's Medical School as a student of the 2017 class. He plans to make contributions to the medical field by utilizing his unique academic background that has fostered innovative and problem solving skills, as well as provide exceptional care for any patients seeking his expertise.